Introduction to Andes Superscalar Processors: N15(F)/D15(F)

Driving Innovations™

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2018/7/31

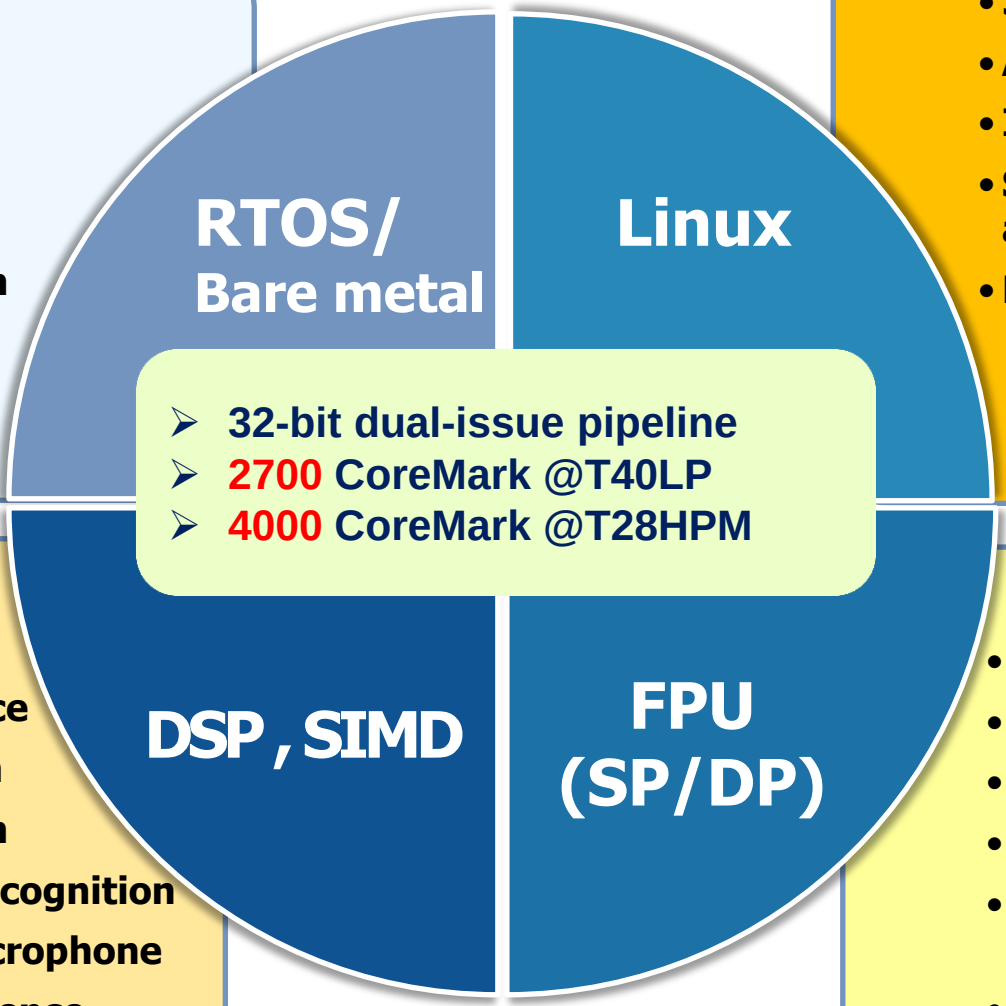
N15(F)/D15(F) - Superscalar Processors

- AndeStar™ V3 architecture
- Four AndesCore™ products
  - **N15** : Baseline ISA
  - **D15** : N15 + DSP extension ISA
  - **D15F** : D15+ Floating point unit
  - **N15F** : N15 + Floating point unit
- 6-stage dual-issue pipeline
  - One instruction from ALU/Multiply/Divide/DSP/Branch/FPU
  - The other from ALU/Load/Store/FPU
- Leading performance
  - **5.41* CoreMark/MHz**
  - **3.36* DMIPS/MHz**

*BSP 4.2.0 toolchain

Applications

- Touch Screen
- PLC
- IoT gateway
- NB-IoT
- Sensor hub
- Home automation
- Wireless vacuum cleaner
- Surveillance



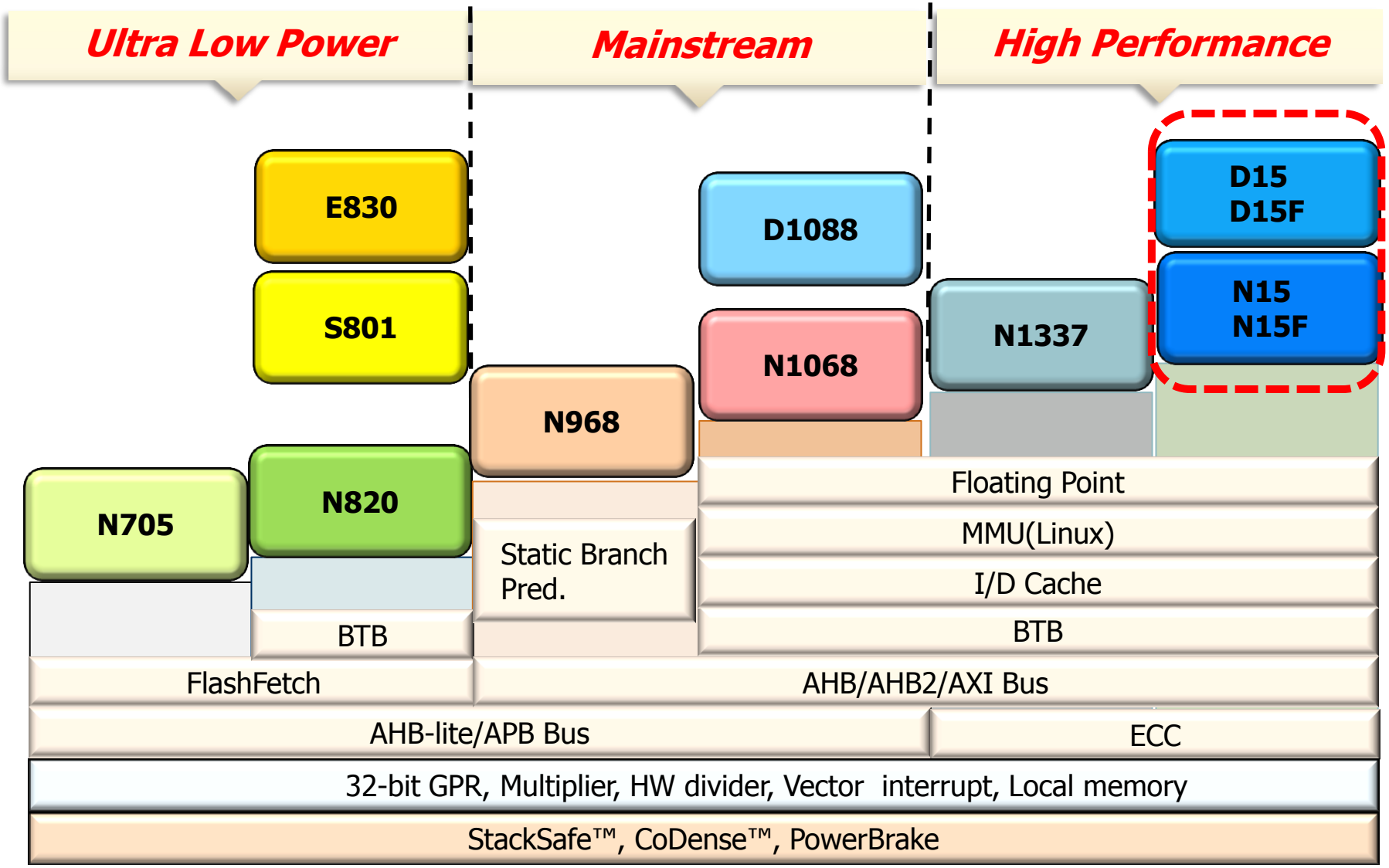
- 32-bit dual-issue pipeline
- 2700 CoreMark @T40LP
- 4000 CoreMark @T28HPM

- 3D printer
- ADAS
- Industrial automation
- Smart home appliances
- HMI control system

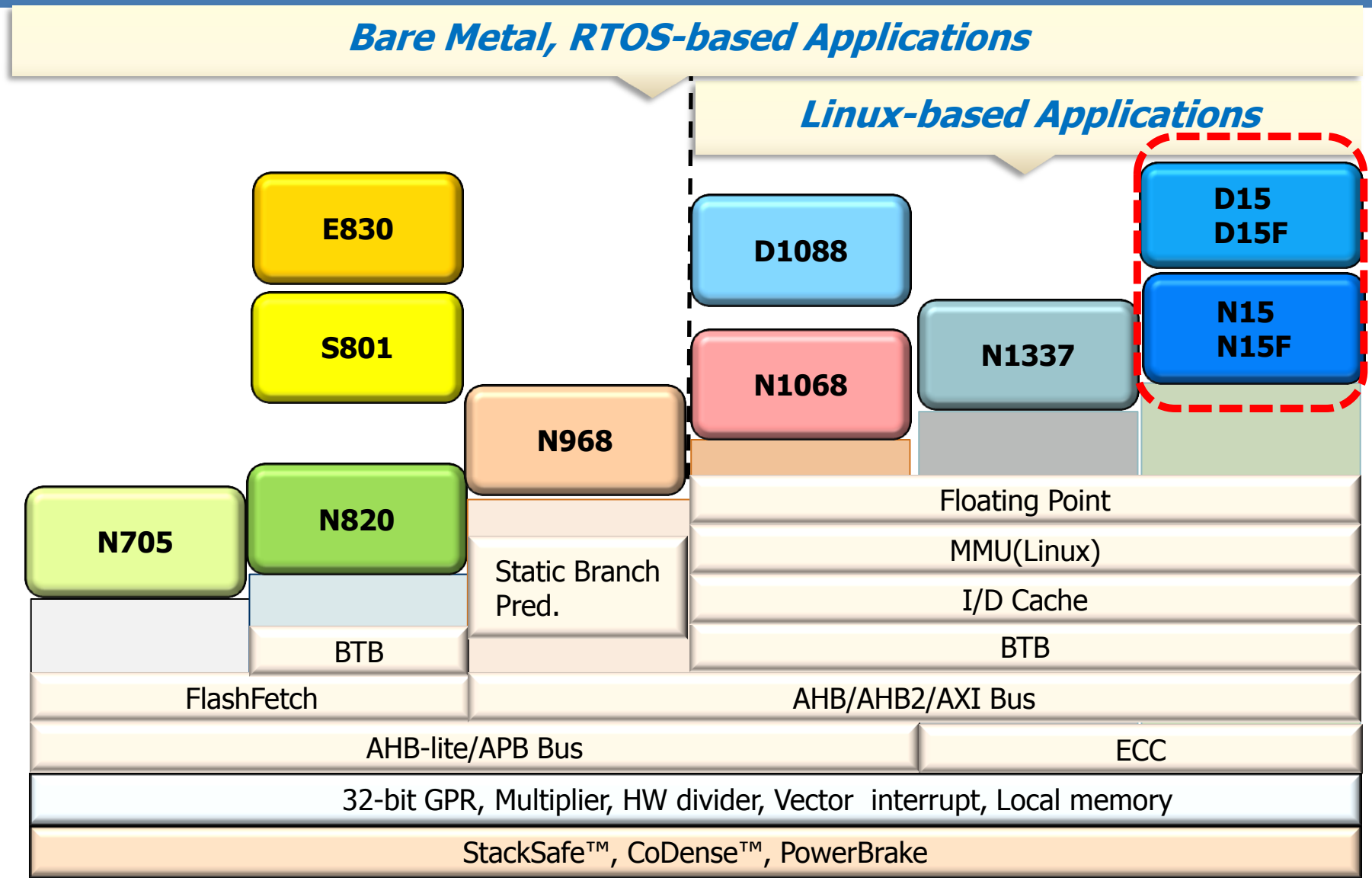
- BT Audio
- Biometrics device
- Computer vision
- Wireless modem
- Voice/speech recognition
- Professional microphone
- Artificial intelligence

- GPS/Beidou
- UAV
- ADAS
- Echo cancellation
- Voice/speech recognition
- Artificial intelligence

AndesCore™ : Product Lineup (V3 Arch.)



AndesCore™ : Product Lineup (V3 Arch.)



Functional Blocks

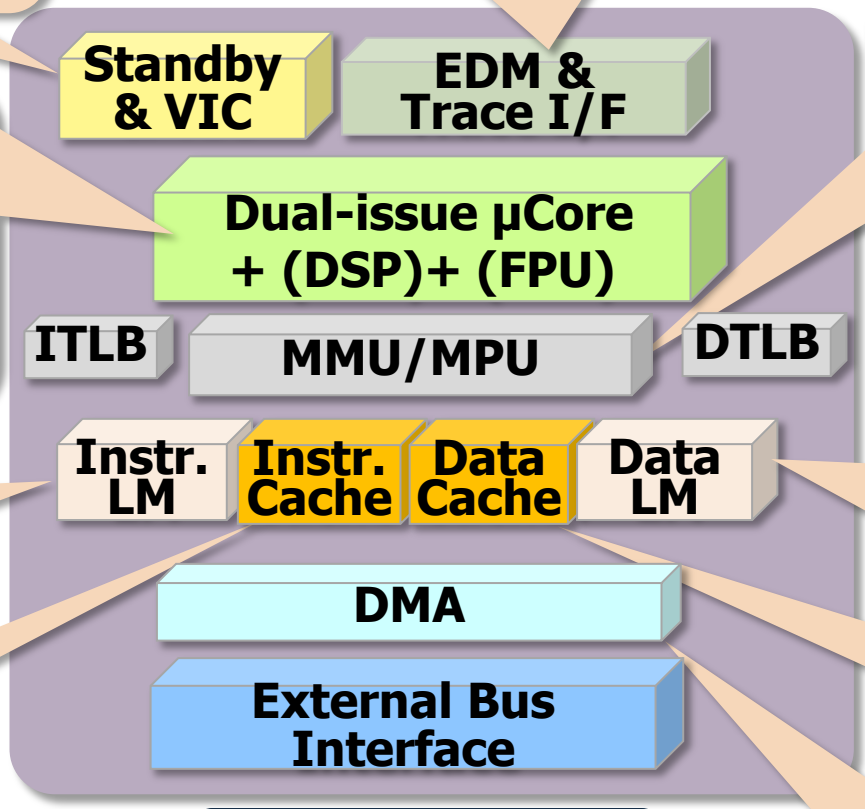
- Pwr. mgmt. instruction
- Powerbrake & QuickNap™ technology
- 32 vector interrupts

- 5-wire JTAG debug I/F
- Trace I/F to Trace module

(EDM: Embedded Debug Module)

- Single-cycle multiplier
- Radix-4 divider
- Dynamic branch pred.
- StackSafe™
- Unaligned LD/ST

- Memory Mgmt. Unit (Linux ready)
- Memory protect regions (8)



- 64-bit
- 1KB to 16MB

(LM: Local Memory)

- ECC (SEC-DED)

- 32-bit x2
- 1KB to 16MB

(LM: Local Memory)

- ECC or parity

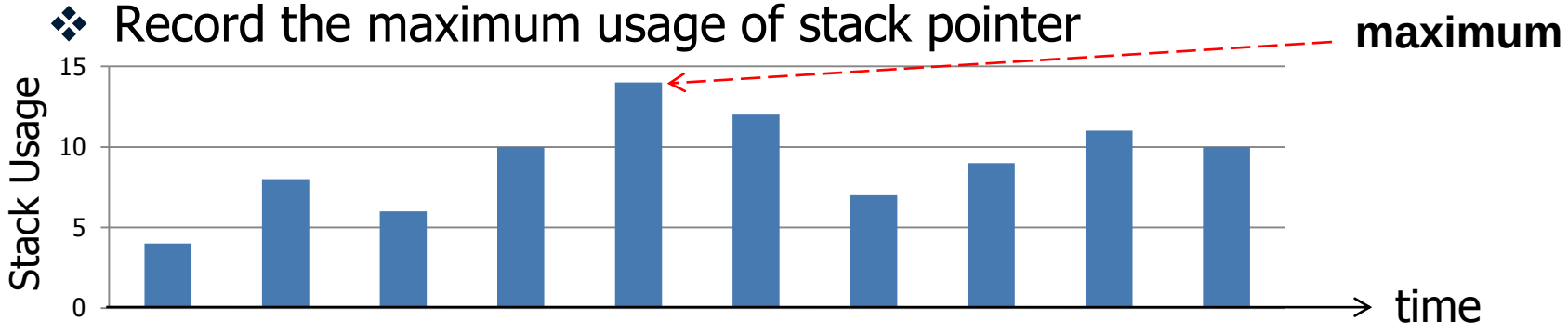
- 4KB to 64KB
- 2-way set assoc.
- ECC

- 4KB to 64KB
- 4-way set assoc.
- ECC or parity

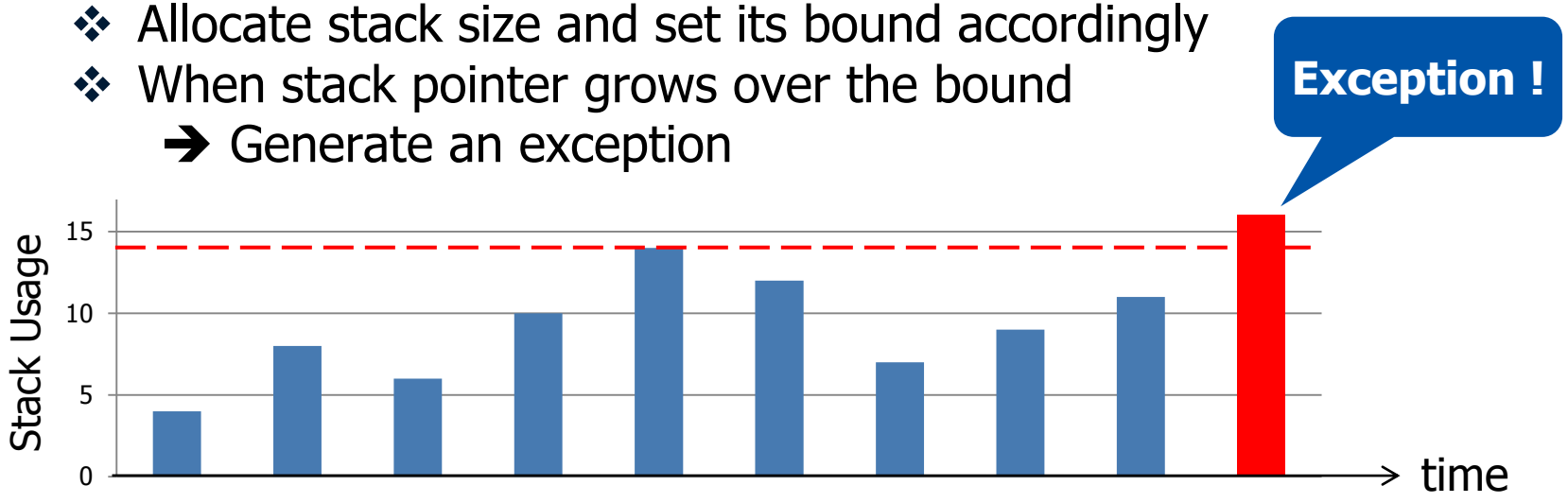
- 1D/2D DMA

StackSafe™ to Protect Stack Usage

- Recording mode:
  - Record the maximum usage of stack pointer

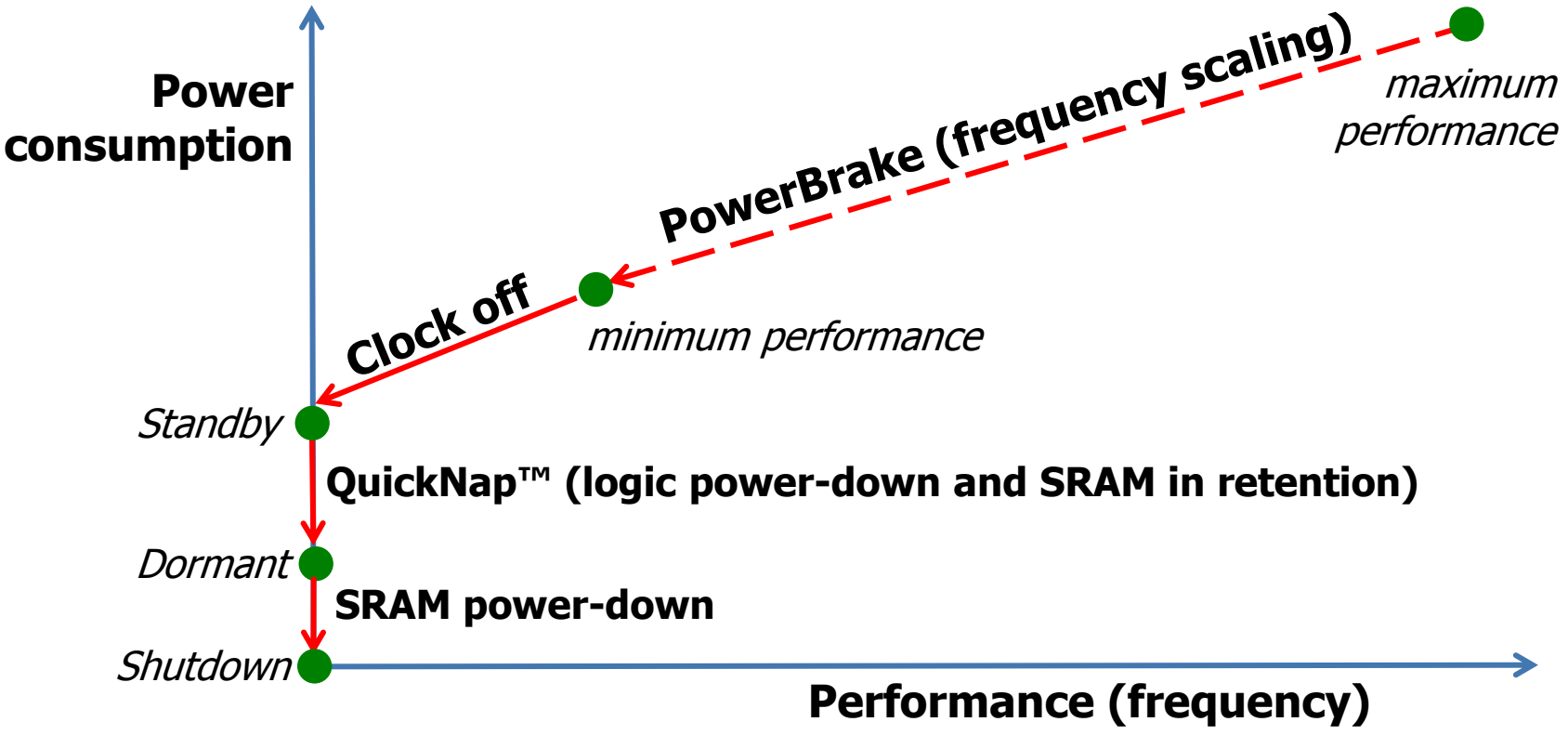


- Protection mode:
  - Allocate stack size and set its bound accordingly
  - When stack pointer grows over the bound
    - ➔ Generate an exception



Power Management

- **PowerBrake** to digitally adjust power (via stalling pipeline)
- **QuickNap™**: logic power-down and SRAM in retention



AndeStar™ DSP ISA Extension (1/2)

- Features:
  - **> 130 instructions**
  - **Saturation and Rounding**
  - Data types: fractional (Q31, Q15, and Q7) and integer (32b, 16b, 8b)
  - 16-bit and 8-bit **SIMD** instructions
    - 16-bit: +, -, x, min, max, abs, clip, compare, <<, >>, signed, unsigned
    - 8-bit: +, -, min, max, abs, unpack, compare, signed, unsigned
  - 64-bit signed/unsigned addition & subtraction
  - **Dual 16x16 Mac**
    - 64 ± = 16x16 + 16x16
    - 32 ± = 16x16 + 16x16
  - Zero-Overhead Loop

AndeStar™ DSP ISA Extension (2/2)

- SW support:
  - Intrinsic functions for using instructions in C.
  - Compiler generation of SIMD instructions based on vector data type.
- >200 DSP-ISA-optimized DSP libraries
  - **110%** performance boost with DSP ISA (average of integer functions)

Andes DSP Library

- Basic math: vector mathematics
- Fast math: sin, cos, atan, atan2, sqrt, etc.
- Complex math
- Statistics: max, min, RMS, etc.
- Filtering: IIR, FIR, LMS, etc
- Transforms: FFT, DCT/DCT4
- Matrix functions
- PID controller, Clark and Park transforms
- MISC: copy/fill arrays, data type conversions, etc.

Floating Point Unit (FPU)

- **IEEE 754 Compliant**
  - **Single** (32-bit) or **Double** (64-bit) precision configuration
  - Register number configuration
    - Single precision: 32
    - Double precision: 16 or 32
  - Support all rounding modes and exceptions
  - Support Flush-To-Zero mode to speedup denormalized number processing
  - Arithmetic (+, -, x, ÷, √), Fused multiply-add operations
  - Compare (==, <, <=, unordered)
  - Format conversion
    - Signed/unsigned integer ⟷ SP/DP
    - SP ⟷ DP
  - Copy/Move (CPU GPR ⟷ FPU GPR, CPU GPR ⟷ FPCSR)
  - Load/Store SP/DP data

AMR-WB Performance

		N10	D10	D15
AMR-WB Encode	MAX	337.07	85.58	58.24
	AVG	289.16	73.13	**49.99**
	MIN	188.50	51.47	33.20
AMR-WB Decode	MAX	75.27	25.21	15.25
	AVG	66.61	21.96	**13.54**
	MIN	54.77	18.22	11.07

The benchmarking numbers are in MCPS. (Million Cycle Per Second)
For all the test vectors, the maximum (MAX), minimum (MIN) and average (AVG) numbers are concluded.
ANSI-C Code for the AMR-WB speech codec:
http://www.etsi.org/deliver/etsi_ts/126100_126199/126173/14.00.00_60/ts_126173v140000p0.zip

Support and Service

Overview of Andes Technology Corporation

Andes Highlights

- Founded in March 2005 in Hsinchu Science Park, Taiwan, ROC.
- Core RD team from **AMD**, **DEC**, **Intel**, **MIPS**, **nVidia**, and **Sun**.
- Just over 140 people; 80% are engineers.
- EETimes' Silicon 60 **Hot Startups to Watch** (2012)
- **TSMC OIP Award** "Partner of the Year" for New IP (2015)
- A founding member of **RISC-V Foundation** (2016)
- **IPO on Taiwan Stock Exchange** (March 2017)

Andes Mission

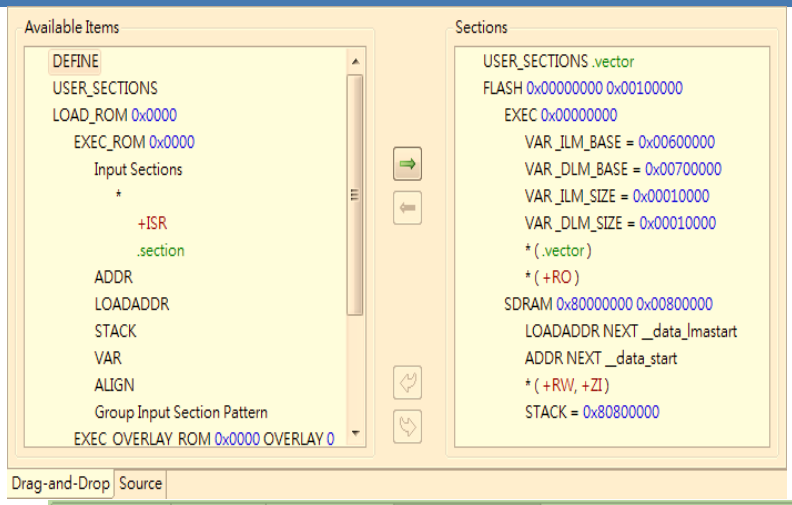
- Innovate **performance-efficient** processor solution for **low-power** SoC

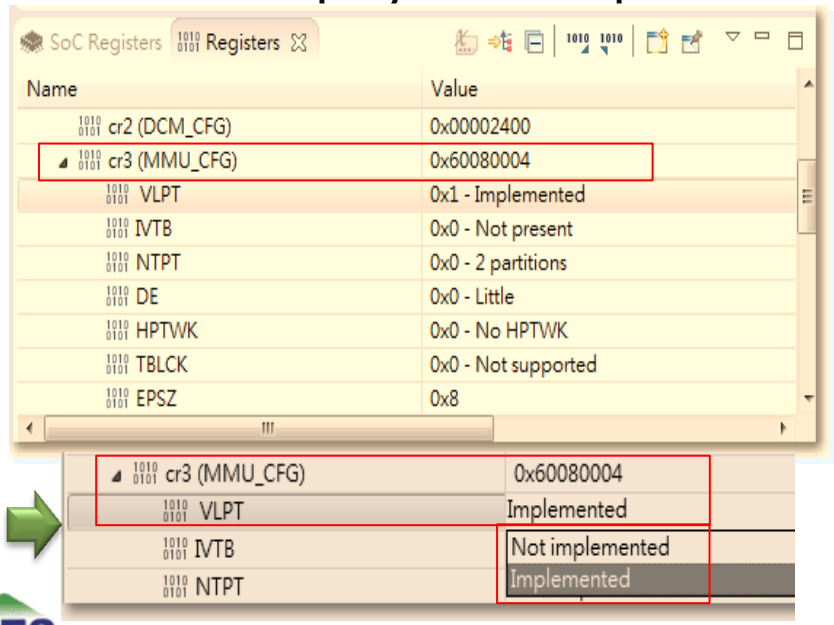
Emerging Opportunities

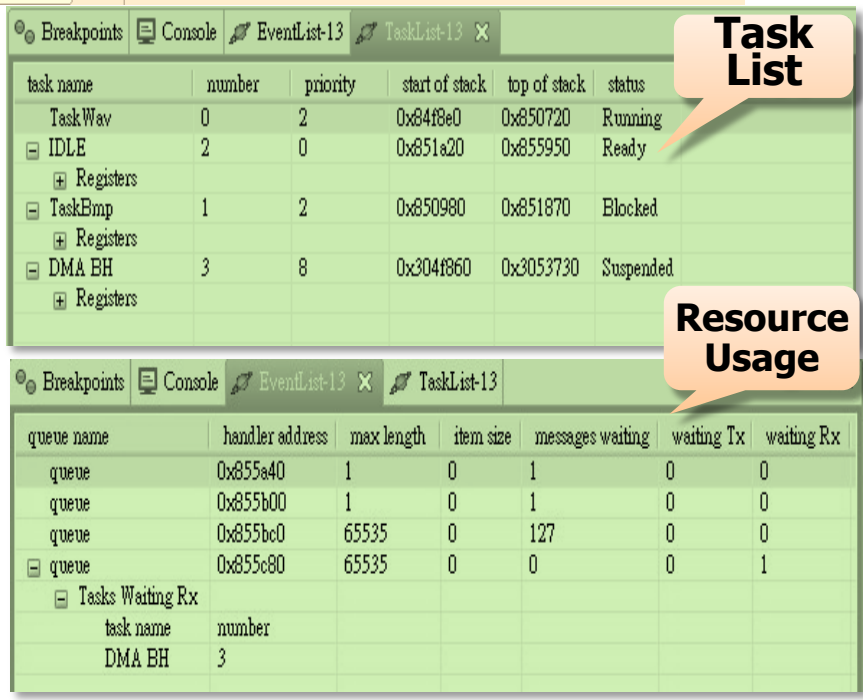
- **Smart** and **Green** electronic devices
- **Cloud Computing** and **Internet of Things**

AndeSight™: Professional IDE (1/2)

- **Eclipse-based**
- **Project Setup:**
  - Meta Linker Script Editor
  - Flash ISP configured through GUI
- **Debug Support:**
  - Script-Based RTOS Awareness
  - Virtual Hosting
  - Register Bitfield Viewing/Update
  - Break-n-Display on Exceptions

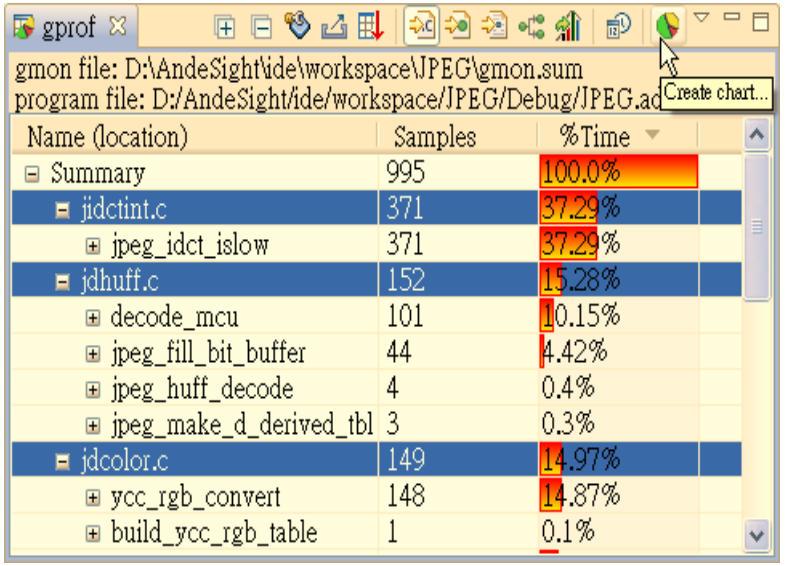


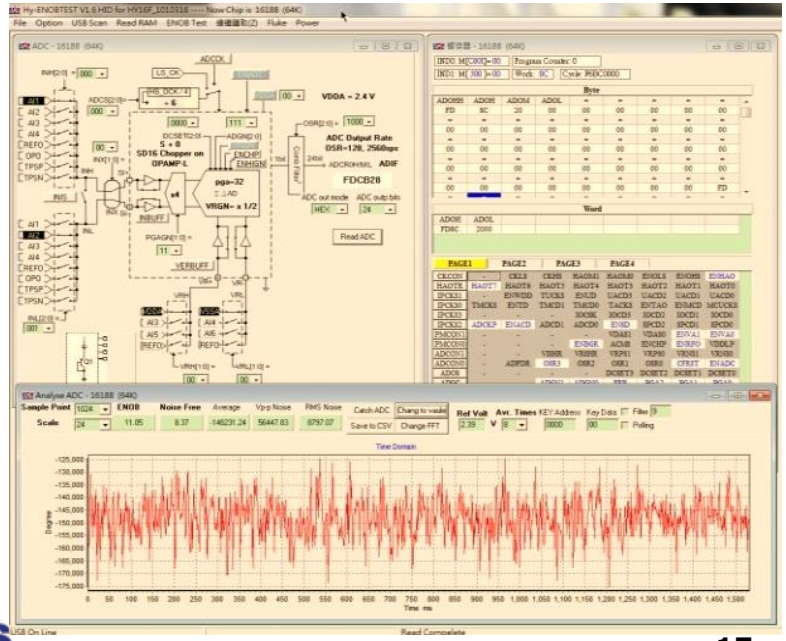


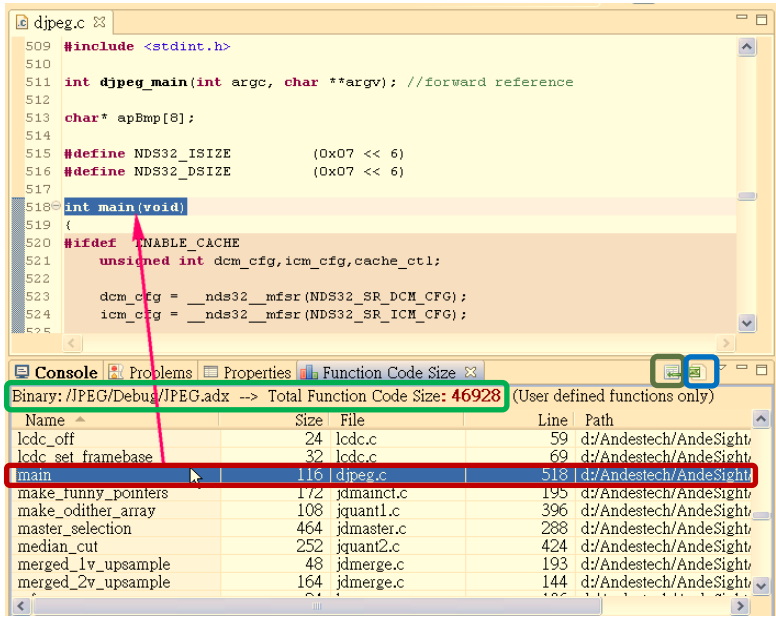


AndeSight™: Professional IDE (2/2)

- **Program Analysis**
  - Function Profiling
  - Performance Meter
  - Code Coverage
  - Function Code Size
  - (Static) Stack Size
- **Debug/Analysis for Arduino**
- **Custom Plugin Intf**





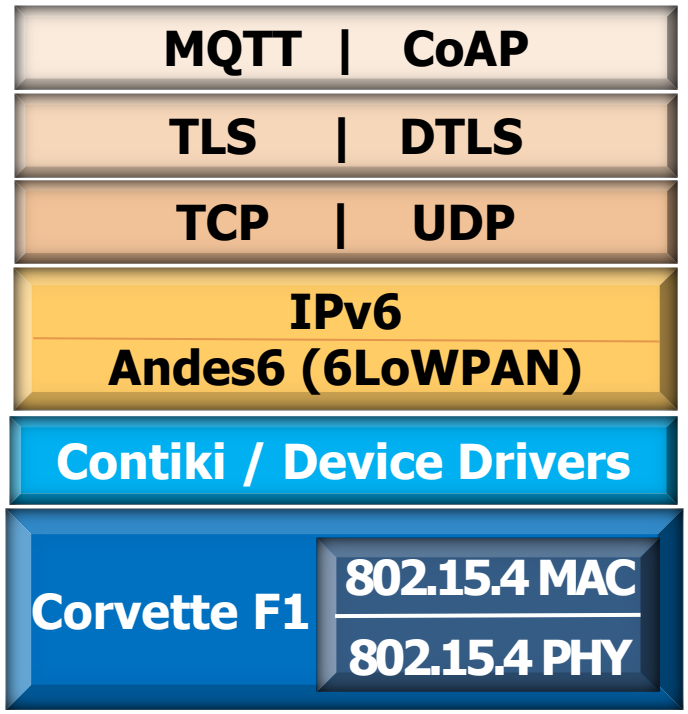


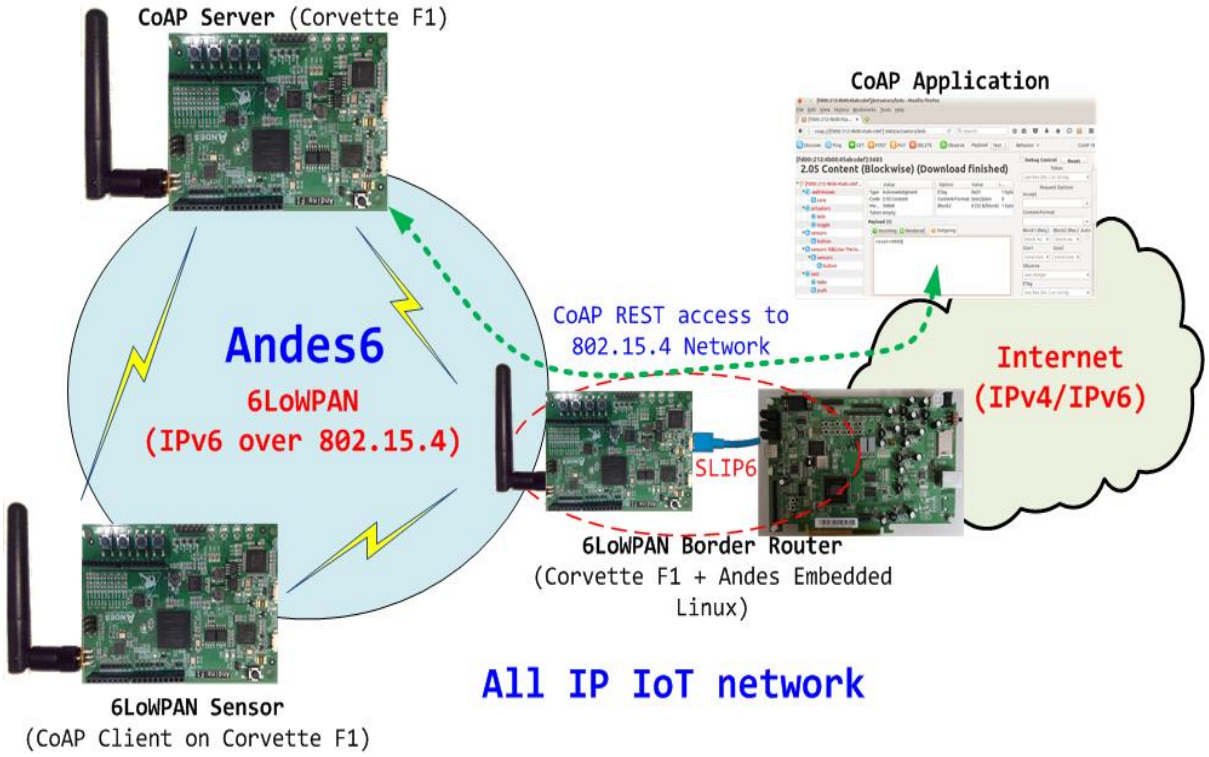
AndeShape™, AndeSoft™ IP Support

- **AndeShape™ Platform IPs**
  - AE300: AXI fabric package for scalable SoC applications
  - AE210P: generic platform IP for micro-controllers
  - AXI Bus Components:
    - AXI bus matrix, bus bridges
    - AXI up/downsizer
  - AHB Bus Components:
    - AHB bus matrix, bus bridge, decoder
    - DMA controller, Local memory bridge
  - APB Bus Components:
    - AHB-APB bridge
    - Serial: I^2C, GPIO, UART, SPI
    - Timer, Watch Dog Timer, RTC
    - Misc.: PIT/PWM, Interrupt Controller
- **AndeShape™ Development Boards**
  - Full-Featured ADP-XC7
  - Compact Corvette-F1 (Arduino-compatible)
    - With 802.15.4 and ICE on board
- **AndeSoft™ SW Stack**
  - Bare metal projects for Andes-enhanced features
  - RTOS'es: FreeRTOS, ThreadX, Contiki, more
  - IoT Stack talking to the Cloud (next page)

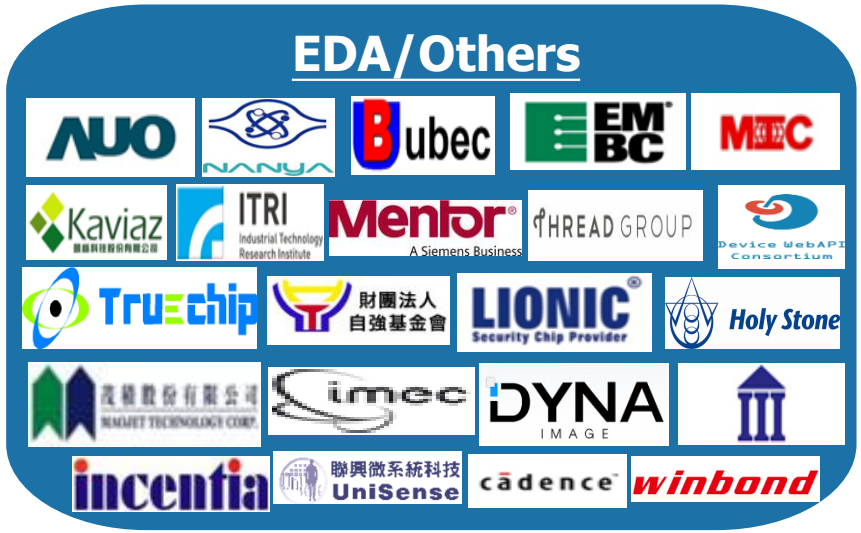
Andes IoT Stack

- **Andes6 connectivity components**
  - Contiki RTOS for OS services
  - An implementation of 6LoWPAN (IPv6 over 802.15.4)
  - Commercial (e.g. InsideSecure) or open source TLS for security
- **Connecting to the Clouds (Microsoft Azure, Acer BYOC)**





Andes Ecosystem



Andes Technical Support

Pre-Sales

- AndesCore™ Introduction
- AndesCore™ Synthesis Report
- Code Size Optimization
- SoC Evaluation Consulting

Post Sales

- Customizable Training Courses
- SoC Design Consulting
- E-service Support

E-service

- A web-based supporting system
- A systematic way to get Andes technical experts' answers
- To help Andes understand your needs and serve you better, you are invited to participate in the Customer Satisfaction Survey when the issue is closed

Concluding Remarks (1/2)

- **WHY Andes**
  - Patented processor architecture
  - Leading performance efficiency
    - Strong on cost performance
    - Strong on power efficiency
  - Intuitive standard SW development tools
  - Comprehensive SW stacks
  - Flexible platform solutions
  - Elite third parties
  - Responsive/experienced customer engineering

Concluding Remarks (2/2)

❖ WHY N15(F)/D15(F)

- **Performance**
  - Extreme HIGH Computing Power
    - 5.41 CoreMark/MHz; 3.36 DMIPS/MHz;
    - 2700 CoreMark in TSMC 40LP process node; 4000 CoreMark in TSMC 28HPM process mode
  - Low Latency and Fast Response Time
- **Power Consumption**
  - Compact Core
  - Optimized Memory Usage
    - Zero-wait memory (on-chip SRAM) + cheap external NOR flash, instead of large external DRAM
- **Easy to Use**
  - Small Real-Time OS, instead of Linux
  - Familiar Development Tools
- **Low BOM Cost**
  - High Level of Integration
  - Core Competence in logic design and algorithm incorporated