

Andes Technology Corporation 2Q18 Investor Conference Report

Driving Innovations™



Stock #: 6533 2018/08/09

Safe Harbor Notice



Except for the historical information contained herein, the matters addressed in this presentation are forward-looking statements that involve certain risks and uncertainties that could cause actual results to differ materially, including but not limited to weather, impact of competitive products and pricing, industry-wide shifts in the supply and demand for semiconductor products, rapid technology change, semiconductor industry cycle, and general economic conditions.

Except as required by law, Andes undertake no obligation to update any forward-looking statement, whether as a result of new information, future events or otherwise.



Agenda

- Overview of Andes Technology Corporation
- Operating Results
- **Product Application**
- New Products and Ecosystems
- Andes Awarded
- Concluding Remarks



Overview of Andes Technology Corporati



Andes Highlights

- Founded in March 2005 in Hsinchu Science Park, Taiwan, ROC.
- Core RD team from AMD, DEC, Intel, MIPS, nVidia, and Sun veterans.
- Under 150 people now; 80% are engineers.
- EETimes' Silicon 60 Hot Startups to Watch (2012)
- TSMC OIP Award "Partner of the Year" for New IP (2015)
- A founding member of **RISC-V Foundation** (2016)
- IPO in Taiwan Stock Exchange (March 2017)

Andes Mission

• Innovate performance-efficient processor solution for low-power SoC

Emerging Opportunities

- Smart and Green electronic devices
- Cloud Computing, Artificial Intelligence and Internet of Things

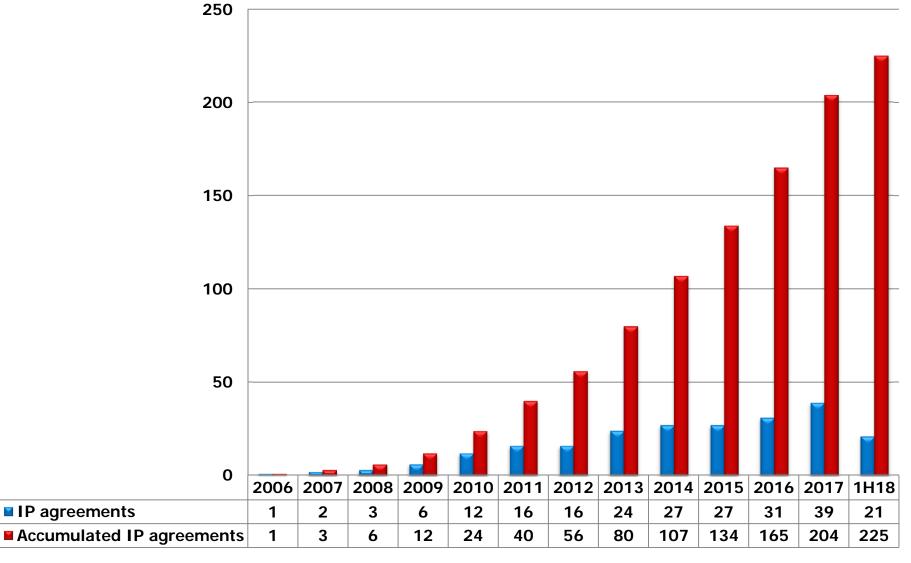


Operating Results



Agreement Growth Analysis







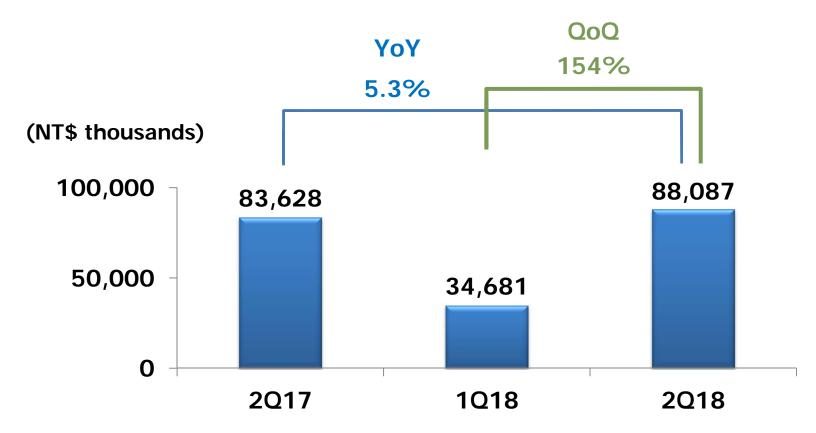
Consolidated Revenue



• 2Q18 Revenue : NT\$88.08M

● YoY: Up 5.3%

● QoQ: Up 154%

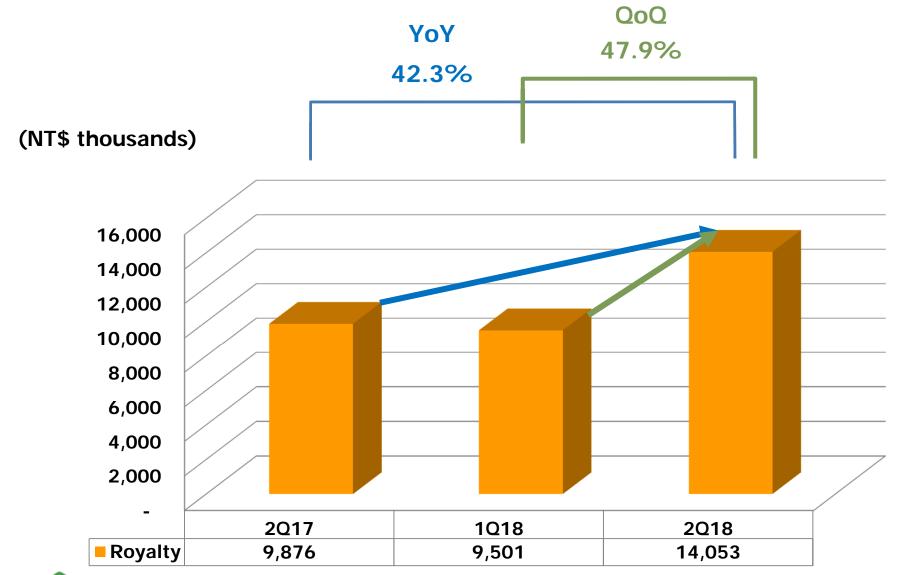




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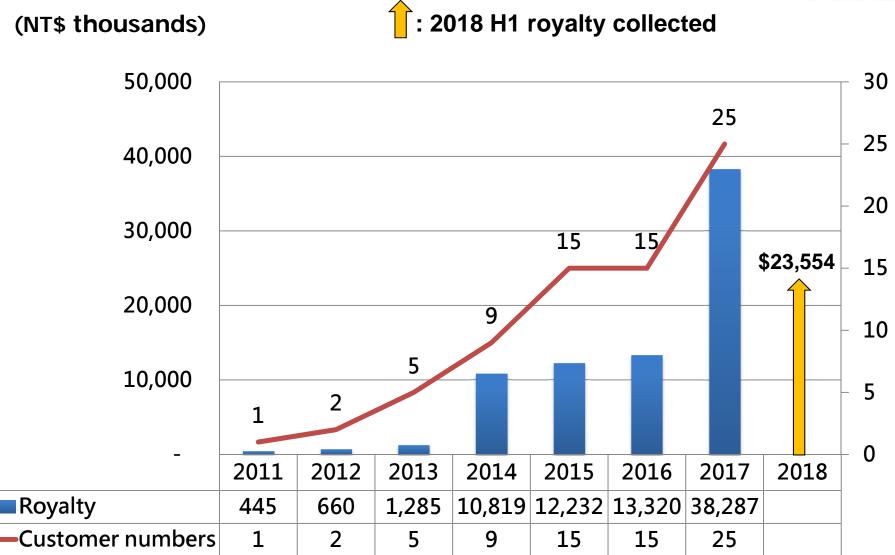
Royalty Analysis





Royalty Analysis



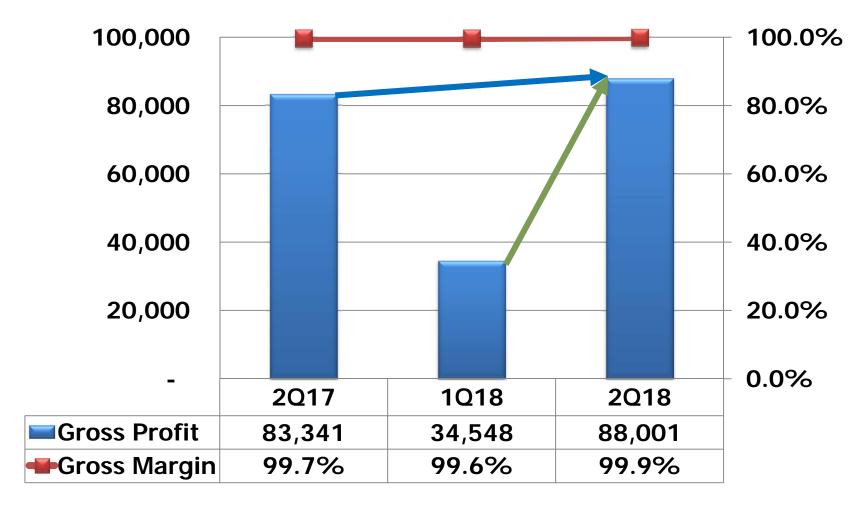




Consolidated Gross Margin



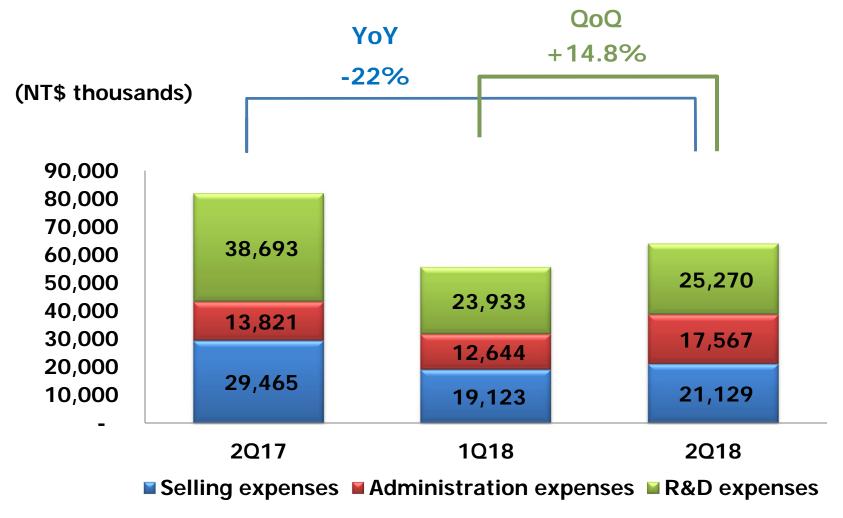
(NT\$ thousands)





Consolidated Operating Expenses

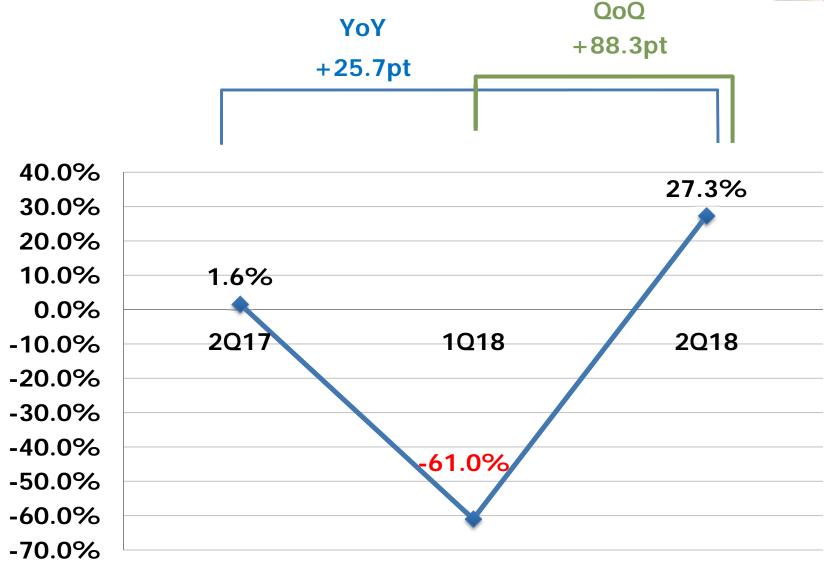






Consolidated Operating Margin

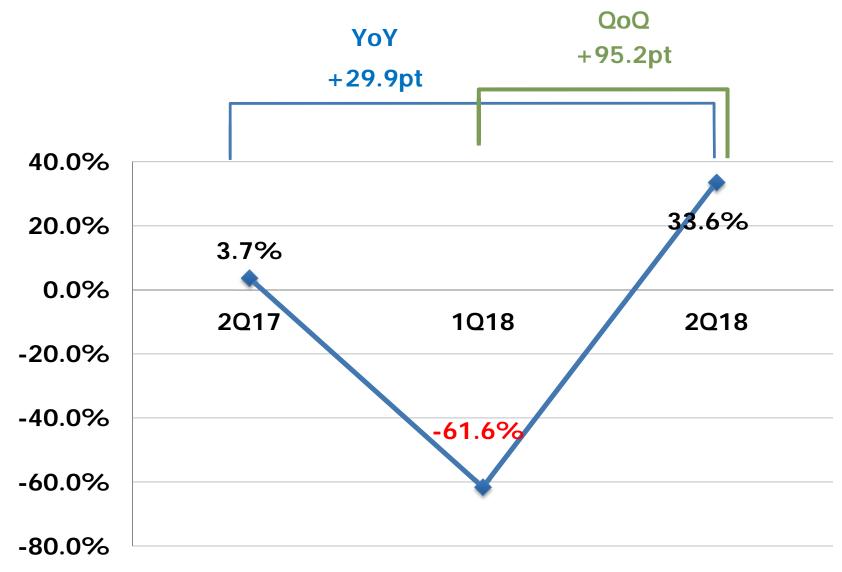






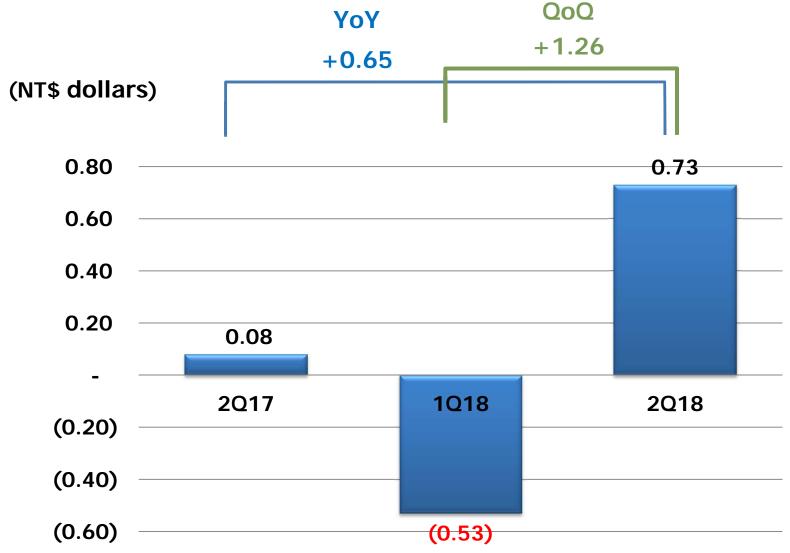
Consolidated Net Profit (Loss) Margin





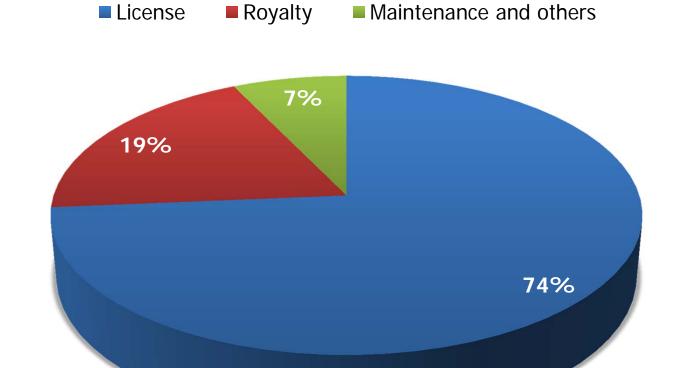
Consolidated Earnings Per Share





1H18 Revenue Analysis by Payment Model

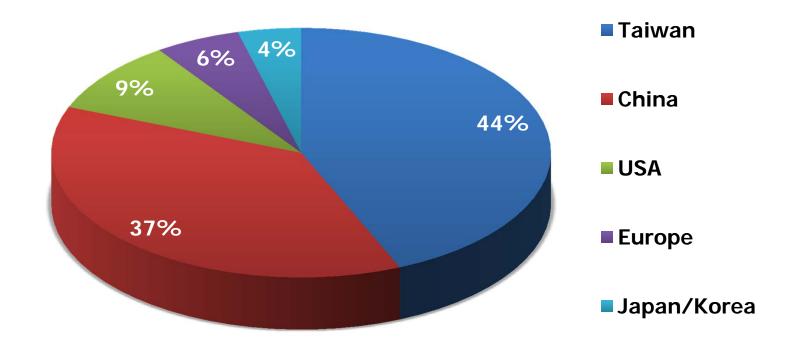






1H18 Revenue Analysis by Region

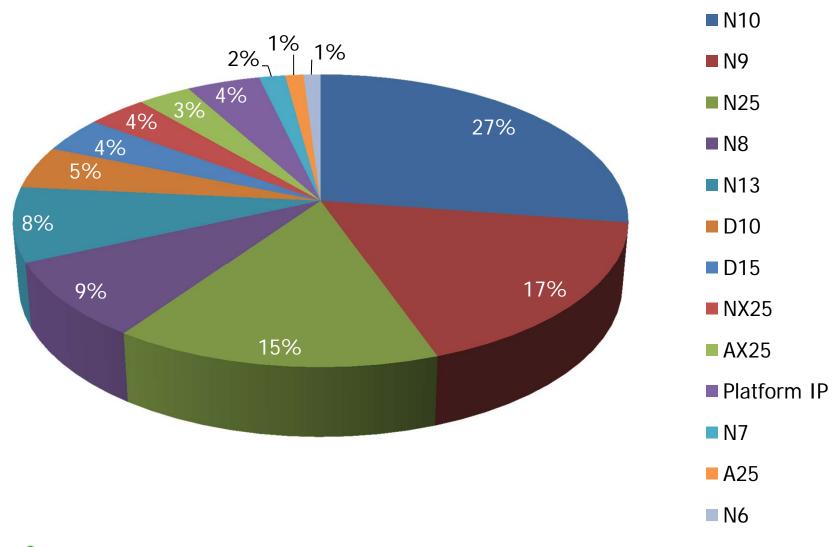






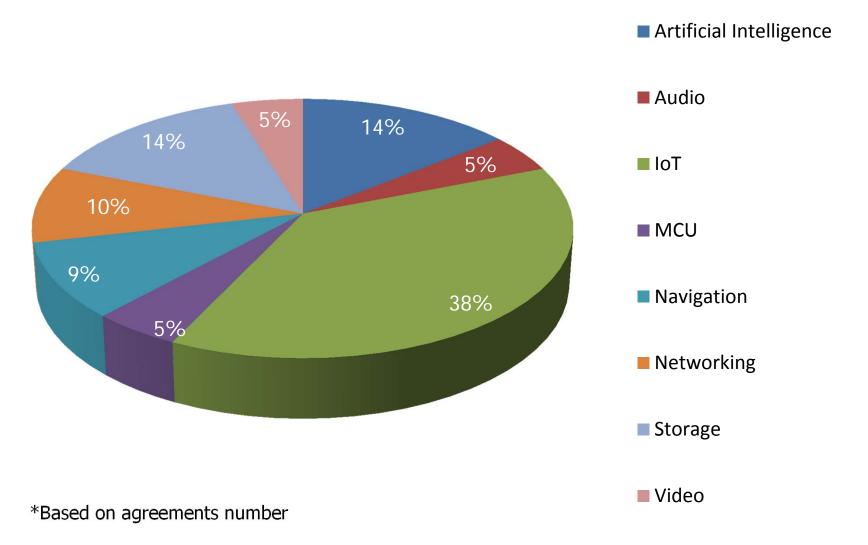
1H18 Revenue Analysis by Product





1H18 Customer Application Analysis







1H18 Design Win

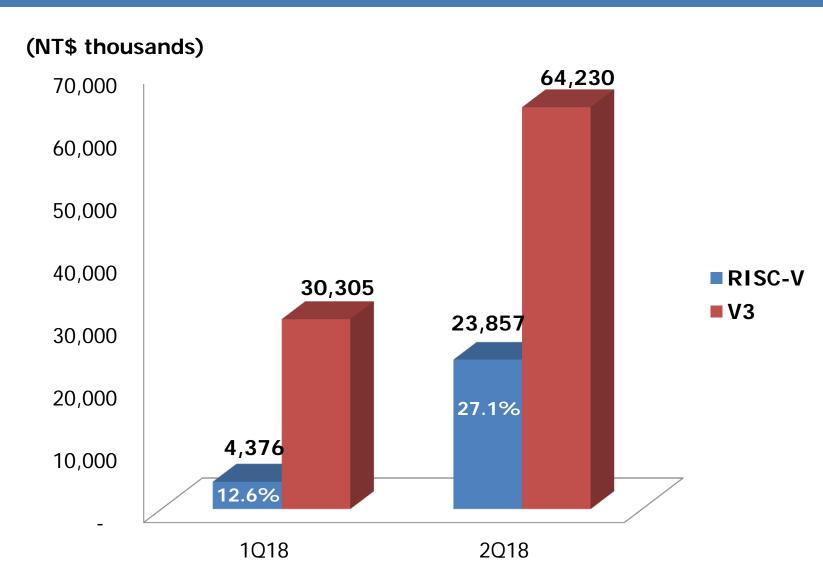


◆ Agreements may sign for H1: 20 ~ 23 reported, now 21

	Jan - June	Subtotal
N7, N8, N9	Mainland x 4, US x 2, Korea x 3, Taiwan x 1	10
N10, D10, N13	Mainland x 4, US x 1, Taiwan x 1	6
D15	Europe x 1	1
N25, NX25, AX25	Mainland x 2, US x 1, Taiwan x 1	4

RISC-V Revenue Share Ramping







Product Application



Rich Customers' Applications

Andes Cone

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- eBook/eDictionary
- Power management
- · Bio-medical device
- CMMB
- MCU
- TCON





- •USB3.0
- •SSD, eMMC
- Anti-virus
- Sensor Hub
- mSATA
- Secure SD
- Fingerprint Recognition



- Wireless display
- WiFi, Bluetooth
- GPS, GPON, NFC
- Gateway/router
- Portable Karaoke
- Sigfox LPWAN
- IoT Cat0 base station
- IoT MCU
 - ESL
- Smart Meter
 Smart Lighting









- Motor Control
- Wireless Charger
- Surveillance
- Barcode scanner
- ADAS
- VEDR
- 4K2K CODEC
- 8K4K CODEC











IoT Application -1







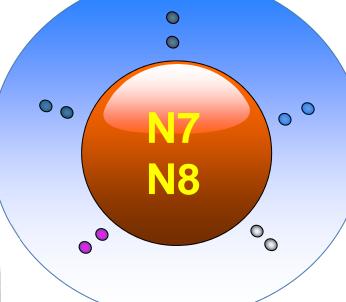
Bluetooth Speaker

Sigfox LPWAN





Healthcare device





Wearable device



Sensor Hub



Electronic price tags



IoT Application -2





Wearable devices





Drone



Portable Karaoke



GPS/Beido in shared bikes







WiFi/GPS/FM/Bluetooth combo



Contactless payment (NFC)



Automotive Applications



- **♦** N13
 - ◆ Calibration of AVM (Around View Monitoring) in NISSAN New X-Trial









- CAR Event Recorder
- ◆ ADAS





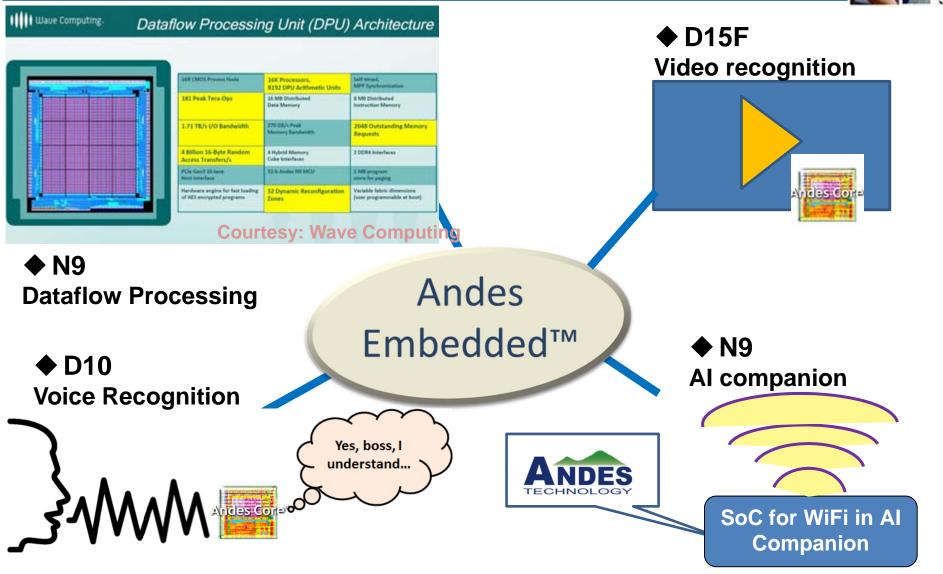






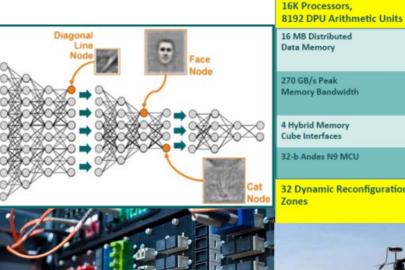
AI Applications

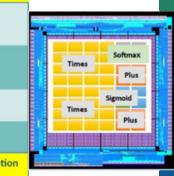




Emerging Applications

- *A
 - Deep Learning
- ❖ Next generation TV
- ❖ Network Engine
 - Router
- Drone
- Robot
- *****
- Many new applications are emerging









New Products and Ecosystems



Product Lines



♦ New Core released in Andes Embedded Forum 2018









V5 AndesCore™ Processors

N25/NX25

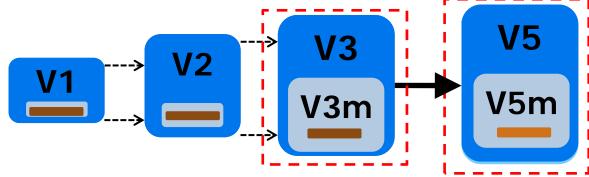
N25F/NX25F

A25/AX25



AndeStar™ V5: New Generation of ISA Kernel





V5m+ more Andes Ext.

RV32/64IMAC+Andes Ext

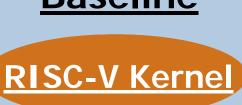
200 Mpiler Opt. COptlor Libraries Secure Rrools

coDensem Stacksafem PowerBrake

Custom Ext. DSP/FP Ext. Security Ext.

Full Feature

Baseline





AndesCore[™] V5 families





Ultra Performance

Enhanced Features

Modern Architecture StackSafe™

CoDense™

V5m, 32-bit 5stage, 1GHz, MMU/MPU, PMP, FPU, ACE...

A25*

N25F*bn' V5m, 32-bit 5-stage, 1GHz PMP, FPU, ACE...

N25 V5m, 32-bit

5-stage, 1GHz Compact PowerBrake

AX25*
V5m, 64-bit 5stage, 1GHz,
MMU/MPU, PMP,
FPU, ACE...

NX25F*CE V5m, 64-bit 5-stage, 1GHz PMP, FPU, ACE...

> NX25 V5m, 64-bit, 5-stage, 1GHz Compact

> > Compact

Next
Generation
V5 (V5m with
adv. features)

I/D Local Memories

I/D Caches

Branch Prediction

64-bit AXI/AHB

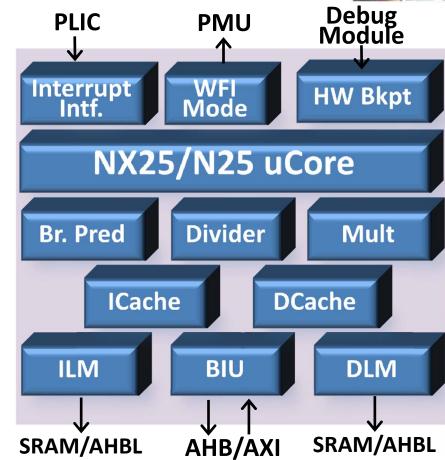
ECC

◆ 28HPC RVT, SS, 0.81V, 0C, with I/O constraints. * Available now



Baseline V5 AndesCore™: N25/NX25

- → Fast-n-small cores for control tasks in storage, networking, AI, and more.
- * N25: 32-bit, NX25: 64-bit
 - From scratch for the best PPA
- AndeStar V5m ISA
 - Superset of RV-IMAC
- **❖** 5-stage pipeline
- Configurable multiplier
 - Sequential or parallel
- Optional branch prediction
- Flexible memory subsystem
 - I/D Local Memory (LM): to 16MB
 - I/D caches: to 64KB
 - Optional parity or ECC
- Bus interface
- JTAG debug module



- ❖ N25 sample config. @ 28HPC:
 - Small: 37K gates, 1GHz (worst)
 - Large: 159K gates, 1.15GHz (worst)



New V5 AndesCores Coming this Summer



- **4 New 25-series:** maintain the frequency
 - **N25F/NX25F**: N25/NX25 + FP support
 - **A25/AX25**: N25F/NX25F + MMU + S-mode
- High-performance FP support:
 - IEEE754-compliant single/double precisions
 - Multiply, add/sub, multiply-accumulate:
 - ◆ 1-cycle issue rate, 4-cycle latency
 - Divide/sqrt: 15 cycles for SP, 29 cycles for DP
 - ◆ Run in the background
 - Half-precision load/store for machine learning
- *** MMU support:**
 - Supporting SV{32, 39, 48}
 - Page size: {Kilo, Mega, Giga, Tera} page
 - 4- or 8-entry microTLBs (ITLB,DTLB)
 - 4-way 32~128-entry Shared-TLB (STLB)





Andes Position in RISC-V



Complete product portfolio

Reliable RISC-V core IP business partner

RISC-V core that runs Linux

Extreme low power consumption, high computing efficiency

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World's only Customer-Extension
Capable RISC-V Core

RISC-∨



YTD RISC-V Design Win



- NX25: Enterprise SSD (Taiwan)
- **❖** N25, AX25: FPGA for AI(US)
- **❖** N25: AI (China)
- * AX25: FPGA for AI (China)
- Six design service providers joined Andes RISC-V Easy Start Program: US x 2, Korea x 1, China x 1, Taiwan x 2





Summary of AndesCores vs. Competitors



AndesCore™	AndesCore/ Competitor	Competitors
	Power Efficiency ¹ (DMIPS/mW)	
<u>N7</u>	+42%	Cortex-M0+
<u>N8</u>	+43%	Cortex-M3
<u>N9</u>	+43%	Cortex-M3
<u>D10</u>	+48%	Cortex-M4
<u>N13</u>	+185%	Cortex-A5
<u>N13</u>	+45%	Cortex-R4
<u>D15F</u>	+121%	Cortex-M7

^{1.} Power Efficiency is DMIPS/MHz divided by power consumption (mW/MHz) when running Dhrystone.



64 Bit Infrastructure and Eco-System



Processor IP's AndesCore™ NX25 Processor Architecture AndeStar™ V5, V5m

smw.adm \$r1,[\$sp],\$r5,0x0
smw.adm \$sp,[\$sp],\$sp,0x2
addi \$sp,\$sp,-8
sethi \$r1,0x50a
lwi \$r1,[\$r1+#0x98]
mov55 \$r2,\$r0
mov55 \$r0,\$r1
lwi \$r1,[\$r1+#0x8]
addi \$r3,\$sp,12

Standby EDM COP Intf

AndesCore uCore

ITLB MMU/MPU DTLB

Instr LM Data LM Cache

DMA Engine

Bus Interface Unit

Development
Platforms
AndeShapeTM

Development Tools

AndeSight™



SW Stacks AndeSoft™





Two Ecosystems: Andes and Knect.me













Knect.me Ecosystem



Built up Ecosystem <u>knect.me</u> to help IoT Developing

■ to **knect** solutions - Silicon IP's, SW stacks, tools, applications, systems

and products

Includes:

- SoC IP Platforms
- Software Stack
- Development Boards
- Development Tools

❖ To Form a IoT League

■ to **knect** chip vendors, partners, application developers, system vendors

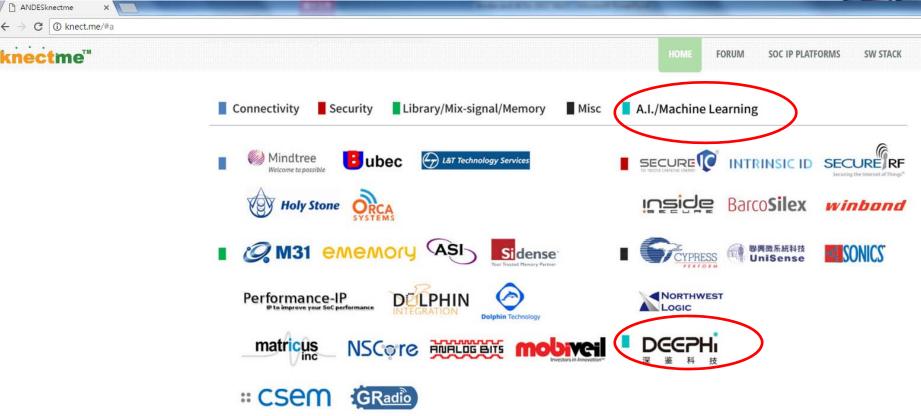




things

Added A.I. to Knect.me Ecosystem





What is "IoT League"? We invite Andes' customers to provide products information which contains AndesCore. IoT League can enhance exposure and reputation in IoT domain. Various applications can help Andes' customers to attract more and more users to adopt their IoT products. Companies in alphabetical order













Andes Awarded



Leader of the Emerging Technology



▶ "2018 Top25 emerging tech solutions provider"

— CIO Advisor Magazine





Concluding Remarks



Andes: Even Better Value in Future

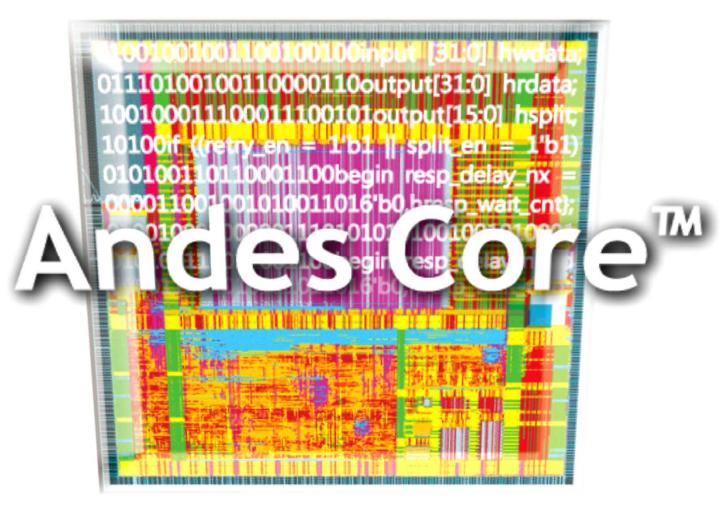


- ❖ Andes aggressively involved in RISC-V Foundation new technology and clusters development, contributing and leveraging RISC-V eco-system. For example, GCC compiler, LLVM compiler, fast interrupt, vector instructions, etc. Andes now leads RISC-V DSP instruction set working group in developing RISC-V Pextension specification discussion and future releasing.
- ❖ Andes has successively signed six contracts with design service houses to authorize ASIC design to embed RISC-V core (Andes RISC-V Easy Start Program). Such alliance program will continue, Andes targets to sign up 20 design service houses worldwide in a few months. These contracts will create a win-win situation for Andes, the design service houses and the end customers.



Thank You!





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Q&A

