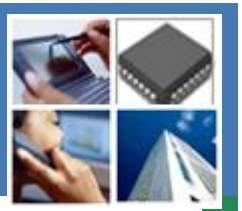
晶心科技股份有限公司
2018年第三季法人說明會

Driving Innovations™

股票代碼: 6533

2018/11/23

投資安全聲明



除簡報內所提供之歷史信息外，簡報事項係屬預測性陳述，受到風險及不確定性因素影響，可能造成實際結果與陳述內容發生不符，這些不確定性因素包括但不限於：天氣、競爭性產品及其定價的影響、產業及市場對半導體產品之供給及需求移轉、新產品大量量產之能力、技術急遽演進、半導體產業景氣以及整體經濟環境之變化。

簡報大綱

- 公司簡介
- 營運成果
- 產品應用
- 新產品及生態系統
- 近期獲獎
- 總結

公司簡介

晶心亮點

- 2005年3月設立於台灣新竹科學園區。
- 核心研發團隊來自於**AMD, DEC, Intel, MIPS, nVidia,** and **Sun**。
- 員工人數約為150人；80%為工程師。
- **EETimes**評為全球60家最具潛力半導體新創公司。**(2012)**
- 獲得**TSMC 2015**年新的 **IP OIP Award** 。
- **RISC-V**基金會創始成員。 **(2016)**
- 股票於台灣交易所掛牌上市。**(2017**年 **3**月**)**

晶心任務

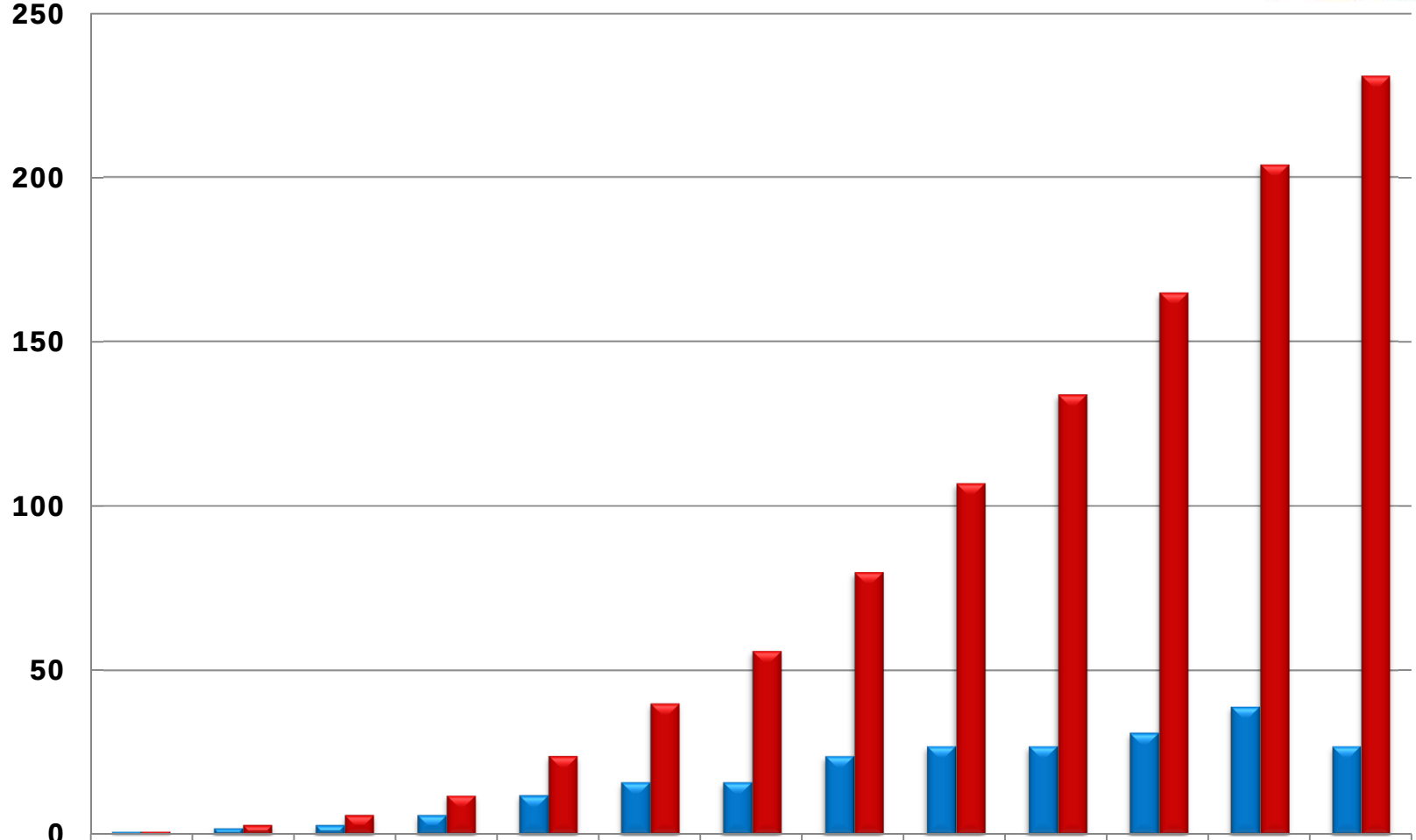
- 創新架構高效能/低功耗嵌入式處理器。

晶心利基

- **智能及環保之電子設備**
- **雲端應用,人工智慧及物聯網**

營運成果

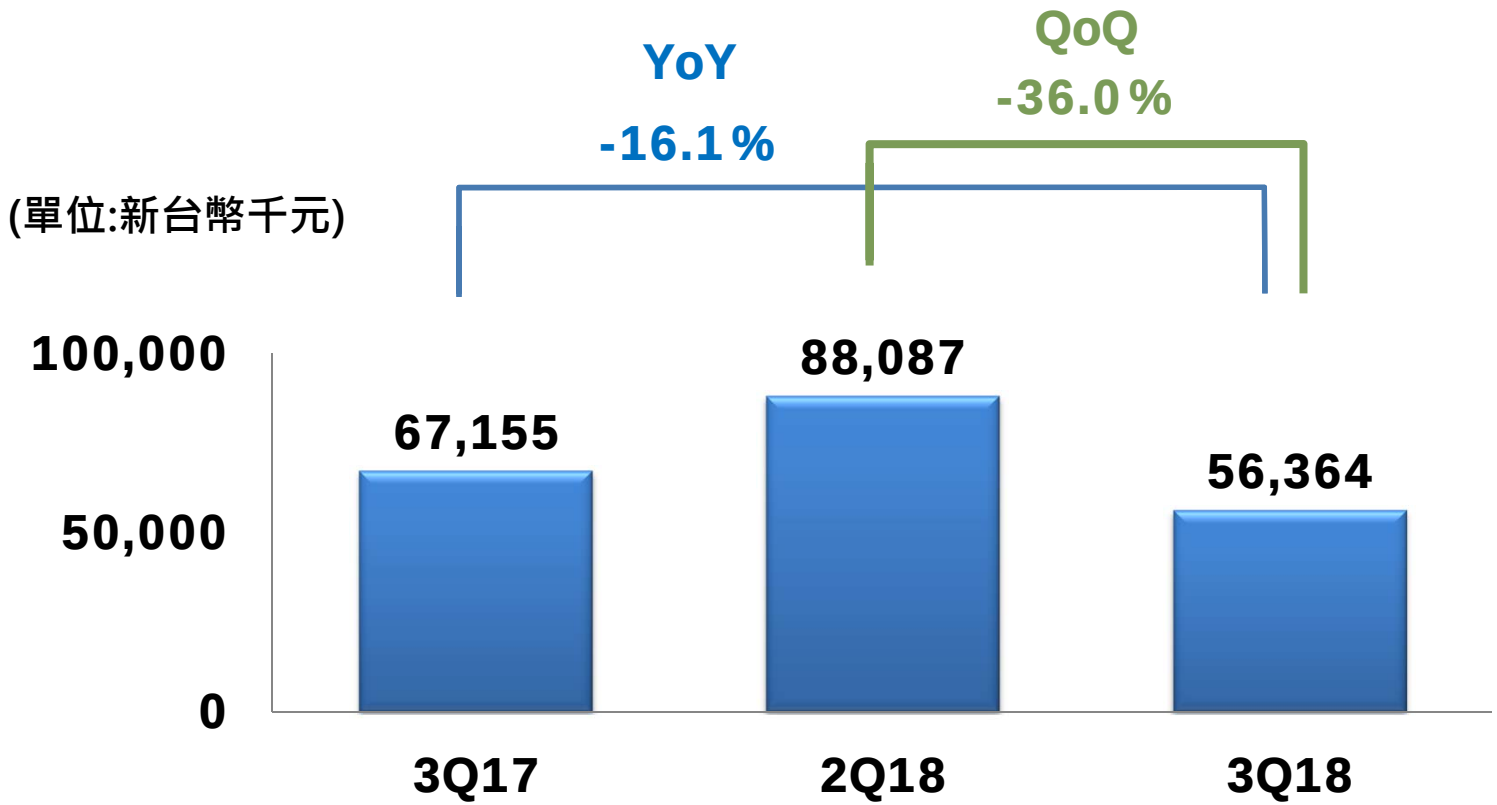
IP 授權合約數成長分析(截至3Q18)



	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	YT3Q18
IP授權合約數	1	2	3	6	12	16	16	24	27	27	31	39	27
累計IP授權合約數	1	3	6	12	24	40	56	80	107	134	165	204	231

2018年第三季營運績效

- 2018第三季合併營收: NT$56.36百萬元
- 年營收成長率(YoY): 減少16.1%
- 季營收成長率(QoQ): 減少36.0%



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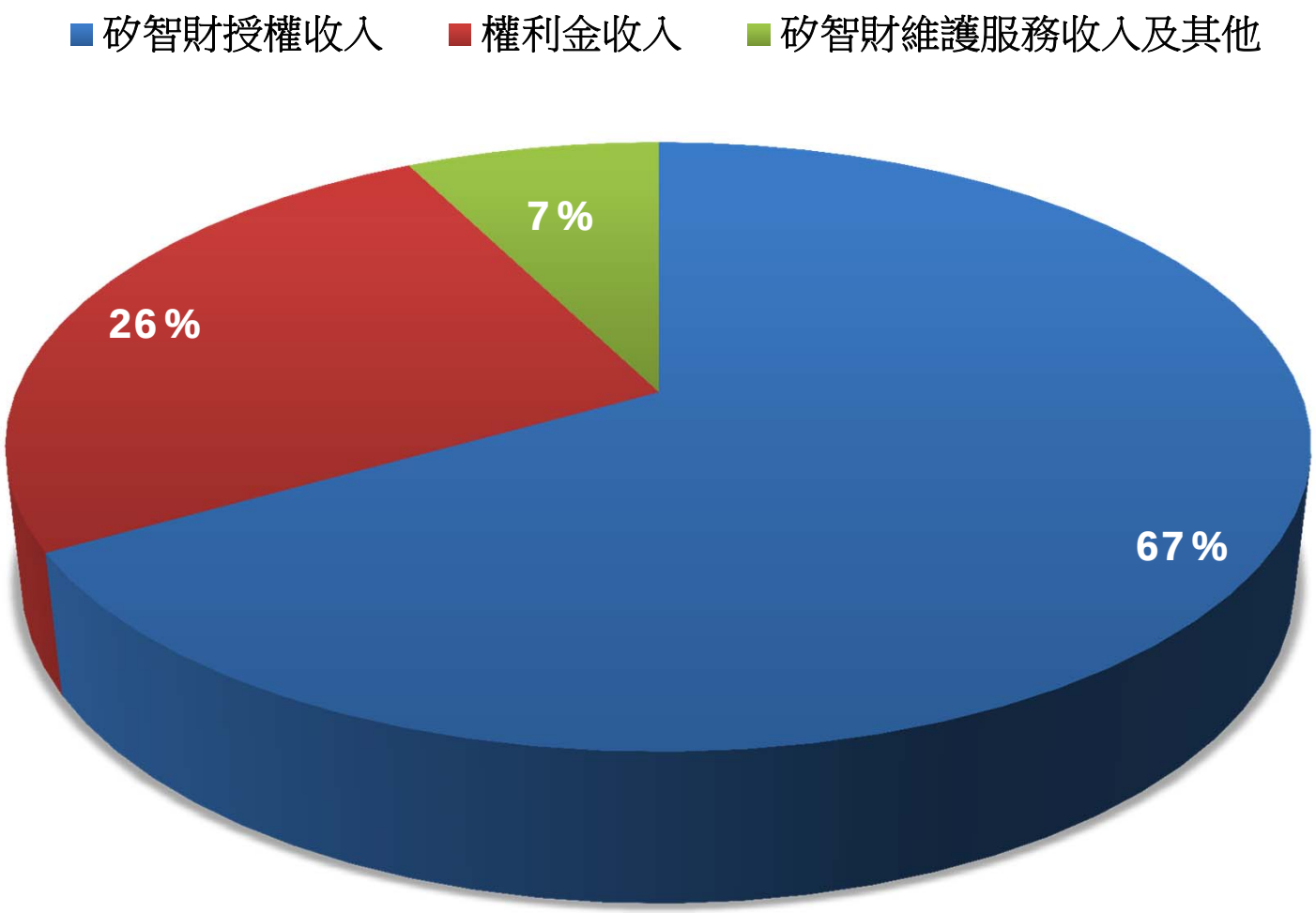
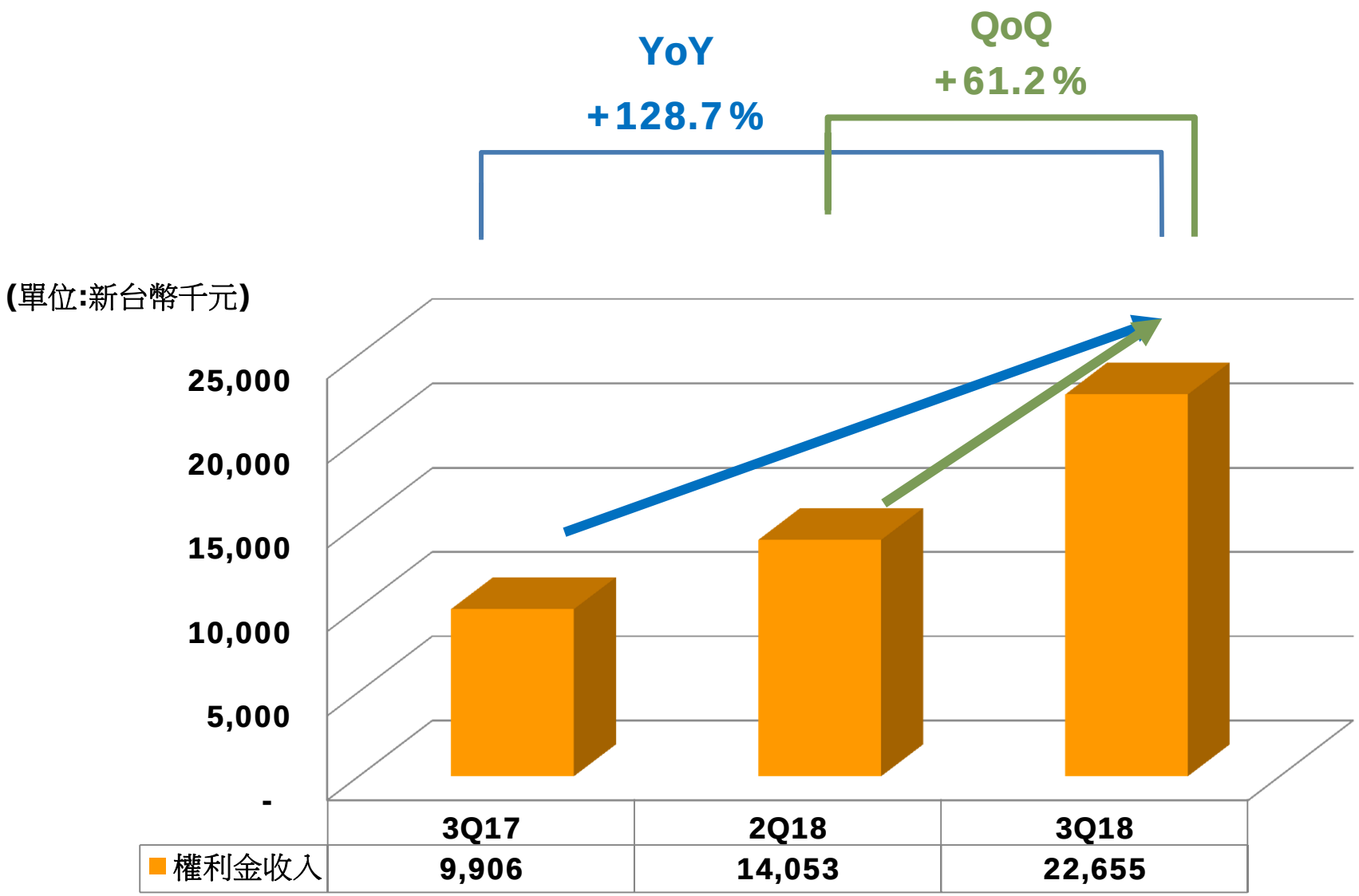
2018年前三季銷售分析-收入模式



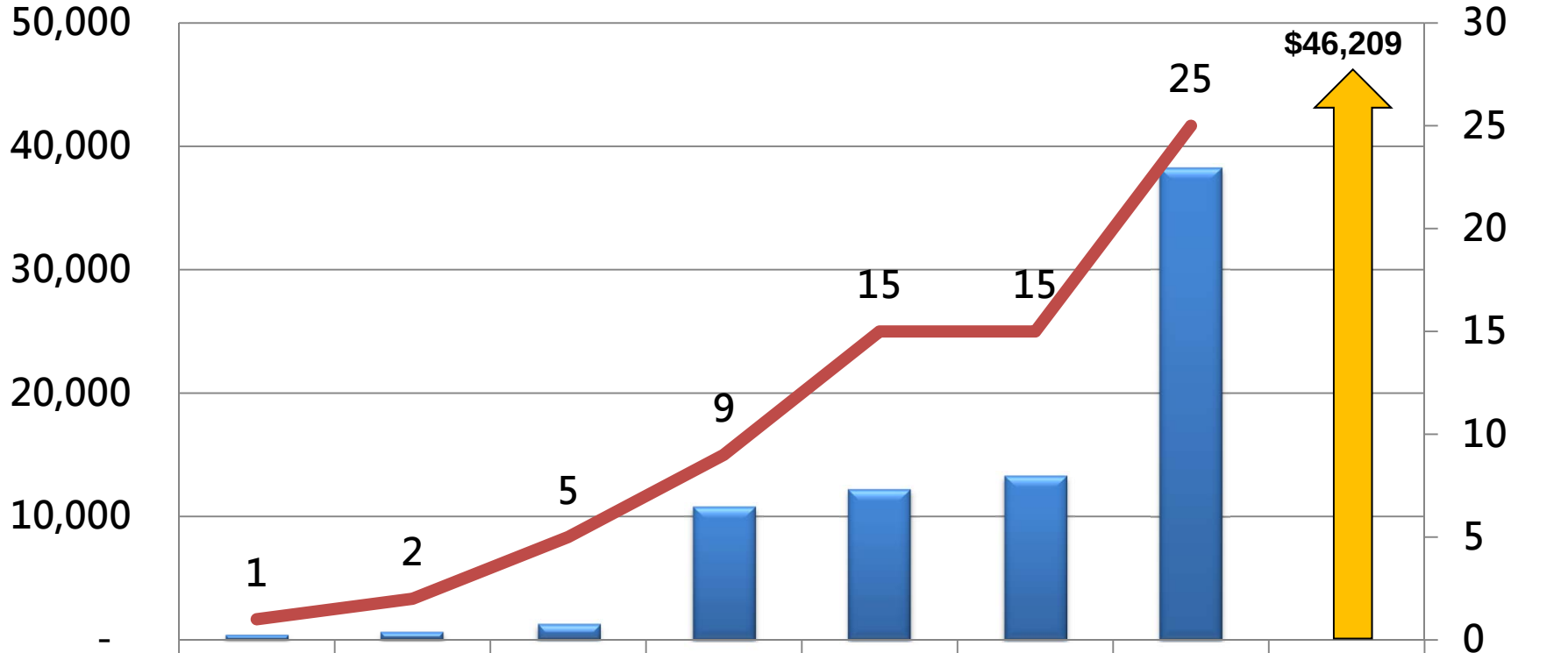
2018年第三季權利金收入



權利金貢獻分析

(單位:新台幣千元)

: 2018 Q1~Q3 royalty collected

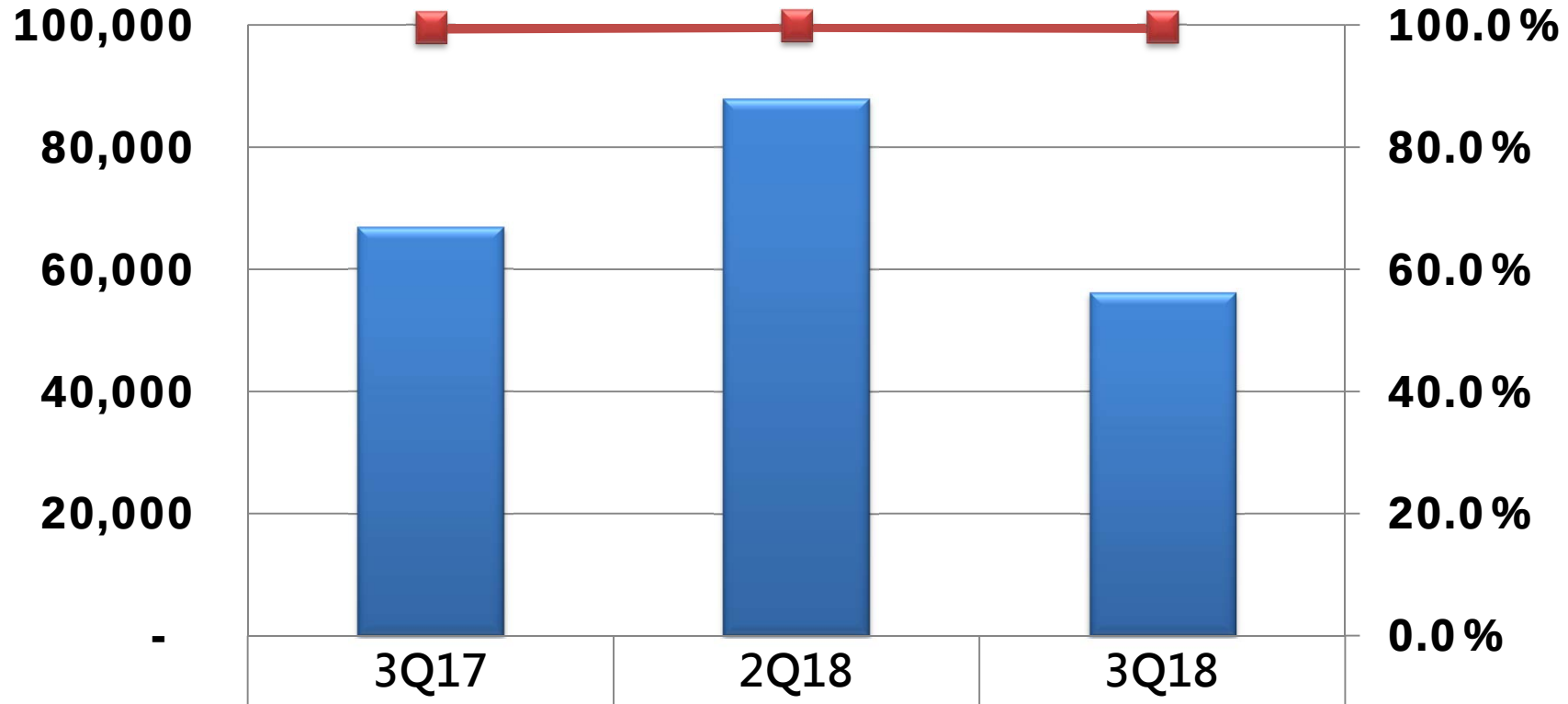


	2011	2012	2013	2014	2015	2016	2017	2018
權利金	445	660	1,285	10,819	12,232	13,320	38,287	
客戶數	1	2	5	9	15	15	25	

(單位:家數)

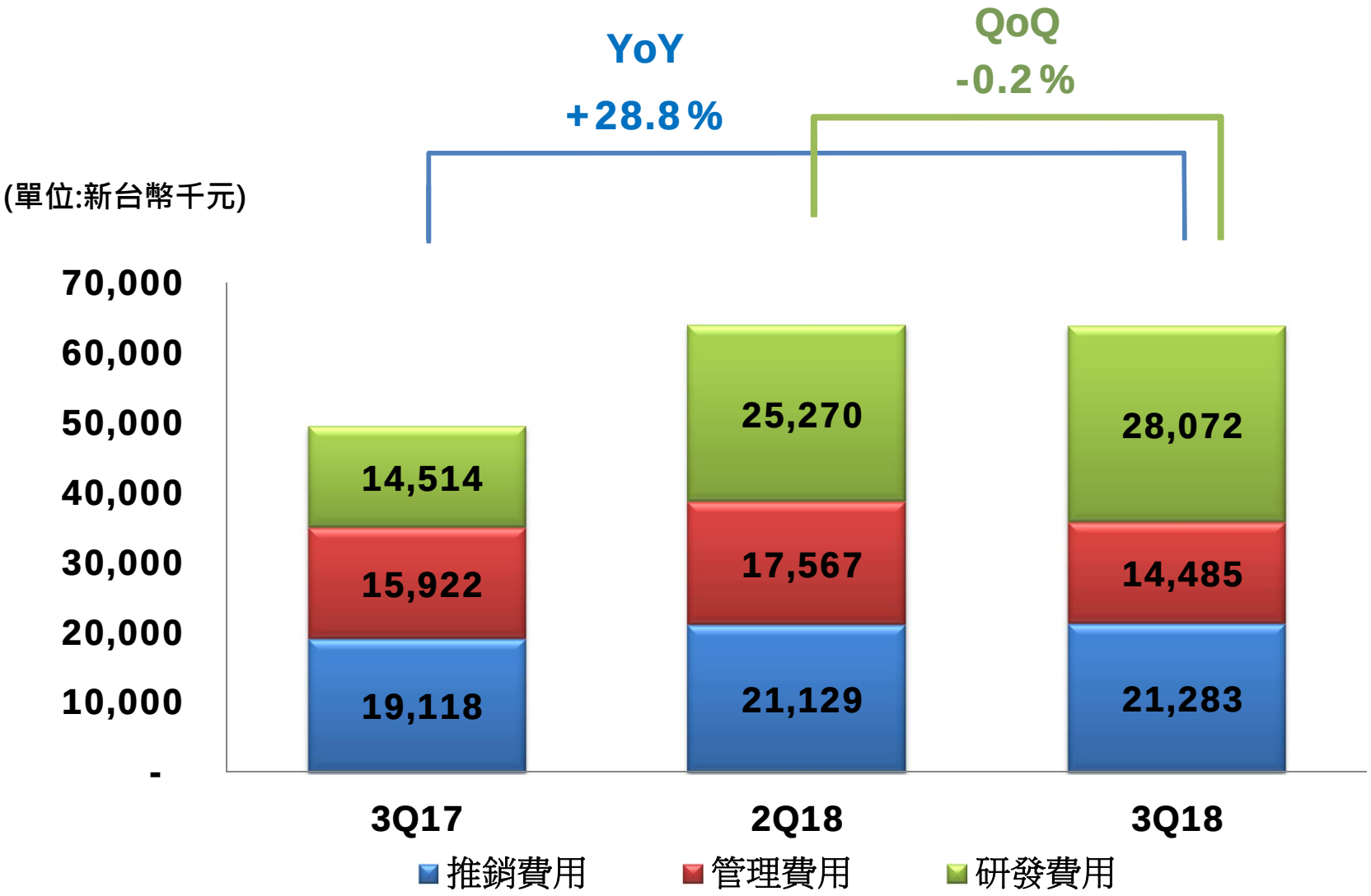
營業毛利與毛利率

(單位:新台幣千元)

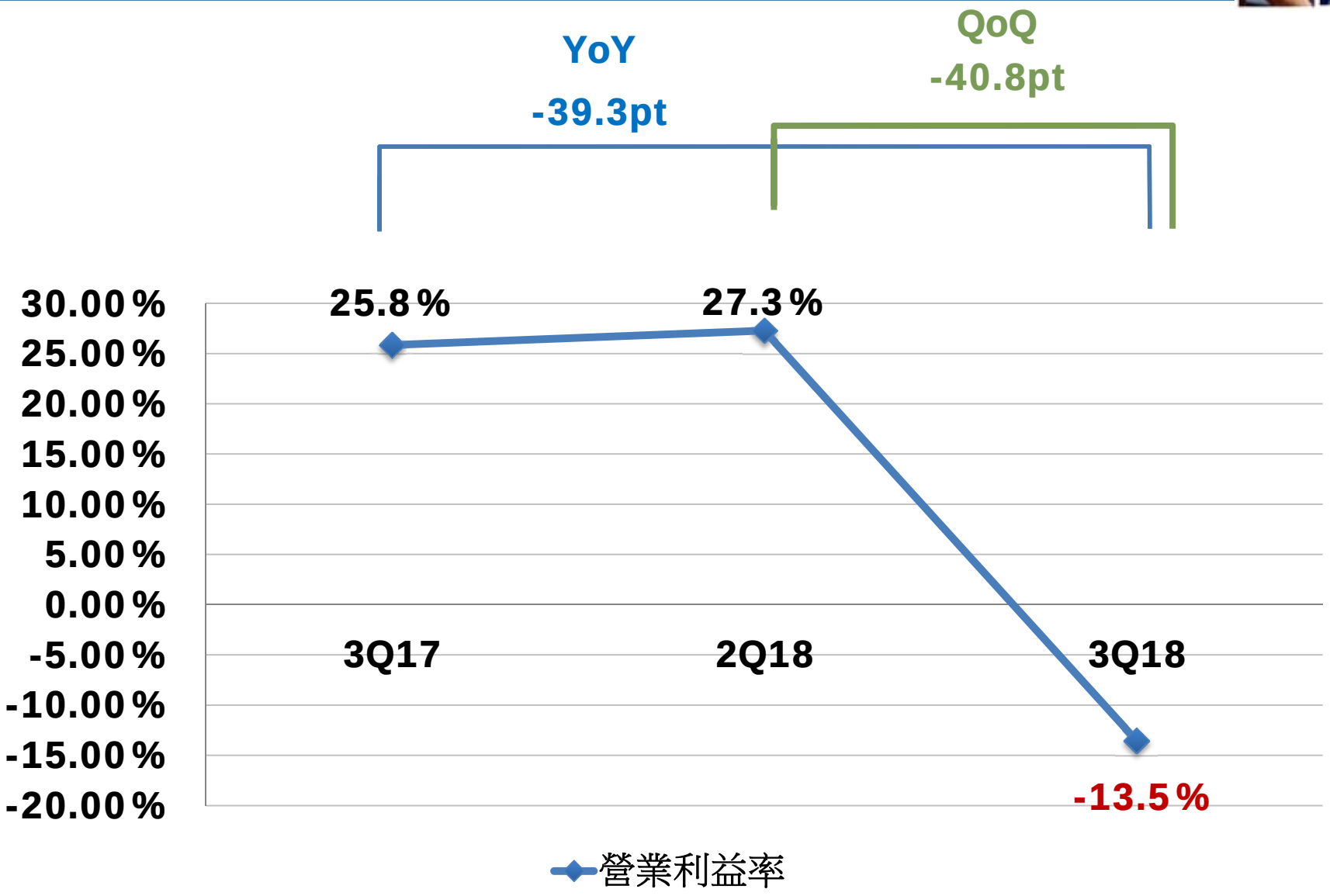


	3Q17	2Q18	3Q18
營業毛利	66,912	88,001	56,217
毛利率	99.6%	99.9%	99.7%

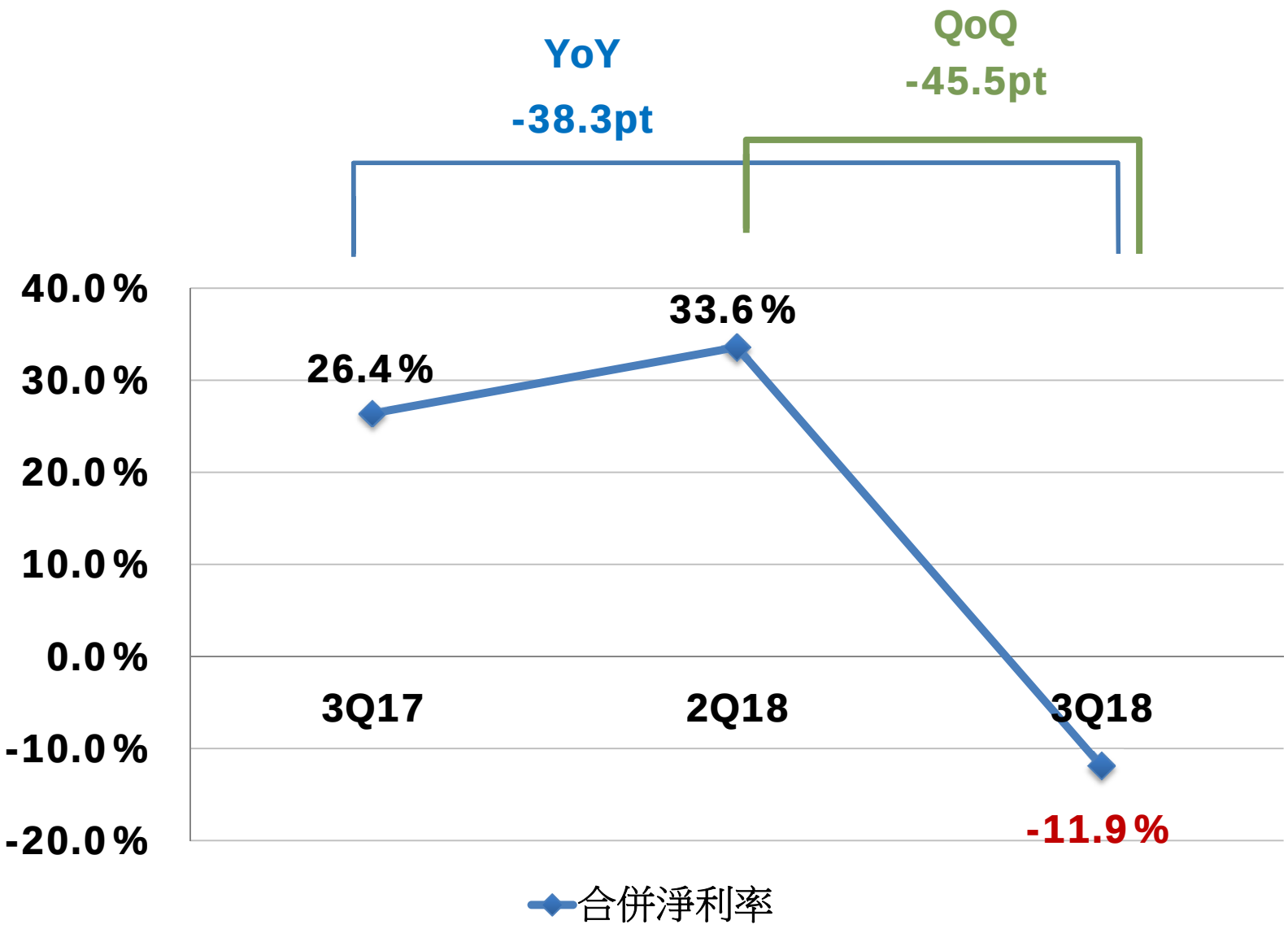
營業費用


YoY
+28.8%
QoQ
-0.2%
(單位:新台幣千元)
70,000
60,000
50,000
40,000
30,000
20,000
10,000
-
14,514
15,922
19,118
25,270
17,567
21,129
28,072
14,485
21,283
3Q17
2Q18
3Q18
推銷費用
管理費用
研發費用

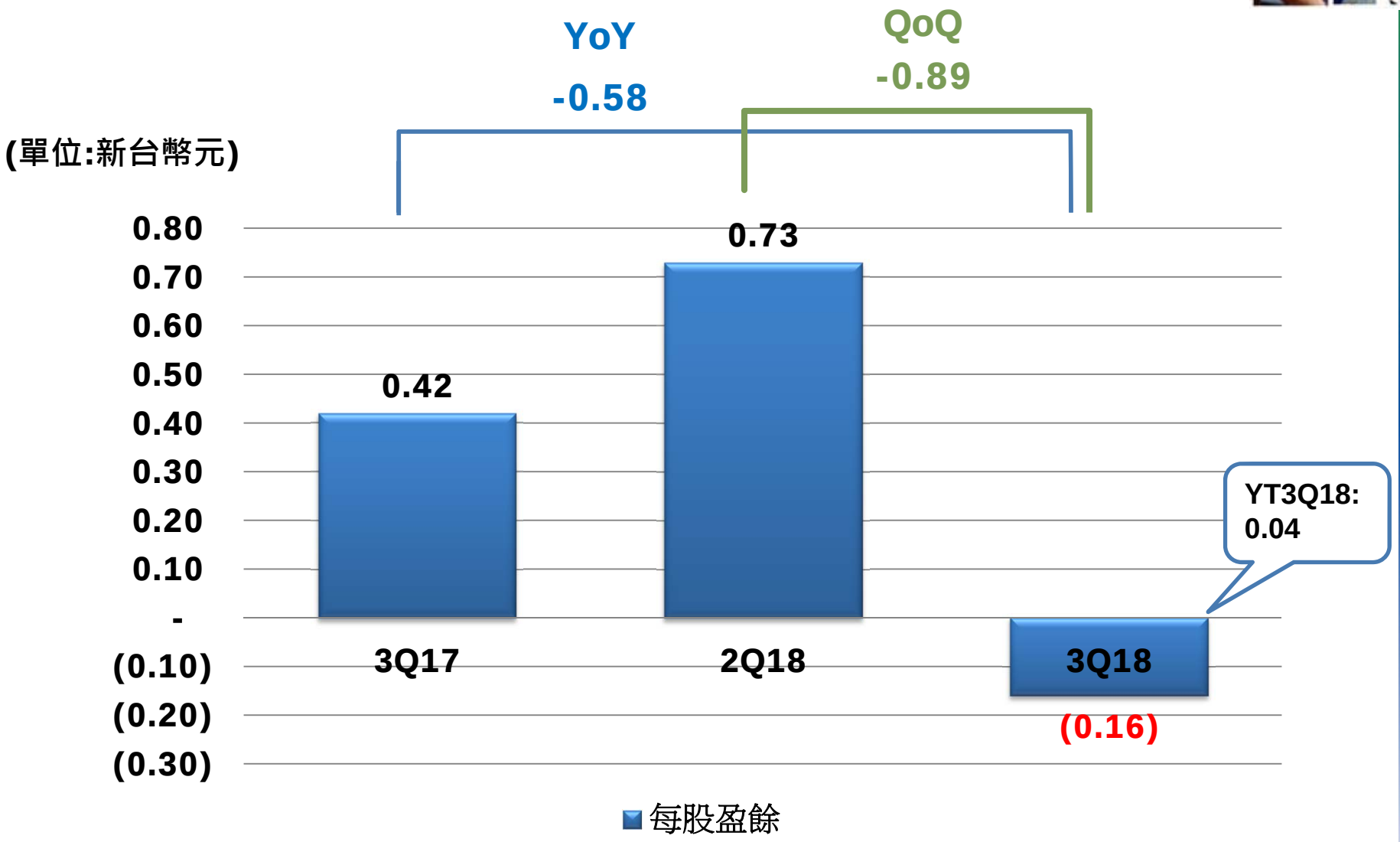
營業利益率


YoY
-39.3pt
QoQ
-40.8pt
30.00%
25.00%
20.00%
15.00%
10.00%
5.00%
0.00%
-5.00%
-10.00%
-15.00%
-20.00%
25.8%
27.3%
-13.5%
3Q17
2Q18
3Q18
營業利益率

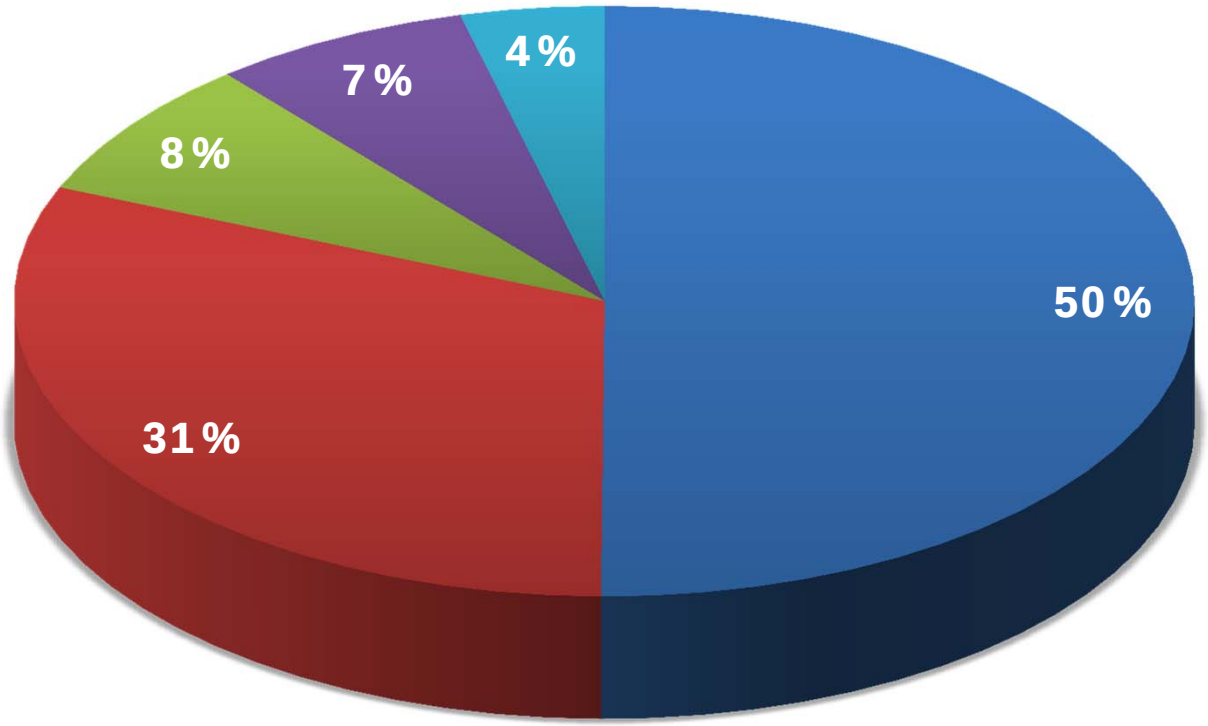
合併淨利(損)率


YoY
-38.3pt
QoQ
-45.5pt
40.0%
30.0%
20.0%
10.0%
0.0%
-10.0%
-20.0%
26.4%
33.6%
-11.9%
3Q17
2Q18
3Q18
合併淨利率

每股盈餘

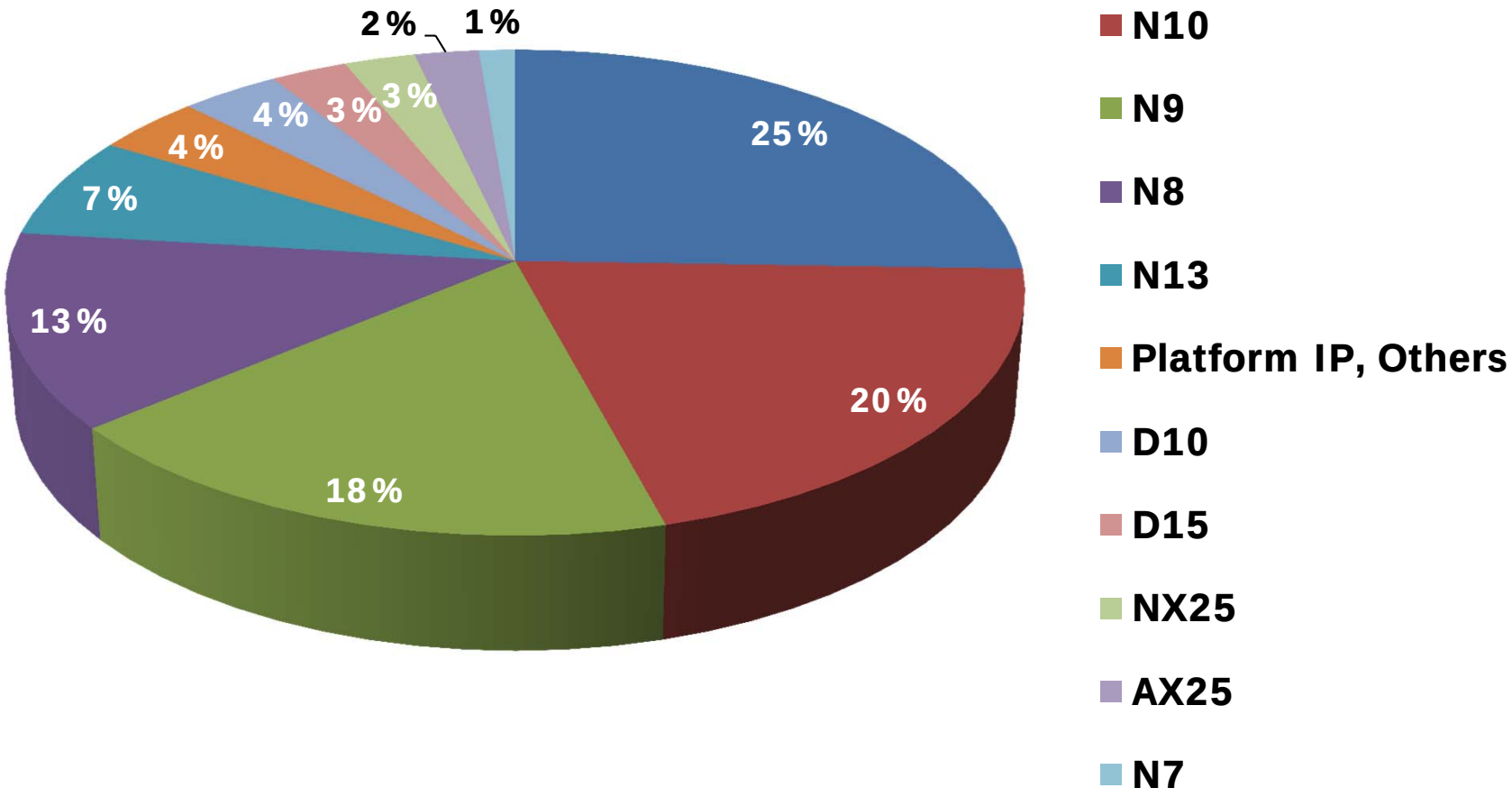

YoY
-0.58
QoQ
-0.89
(單位:新台幣元)
0.80
0.70
0.60
0.50
0.40
0.30
0.20
0.10
-
(0.10)
(0.20)
(0.30)
0.42
0.73
(0.16)
3Q17
2Q18
3Q18
YT3Q18:
0.04
每股盈餘

2018年前三季銷售分析-地區別

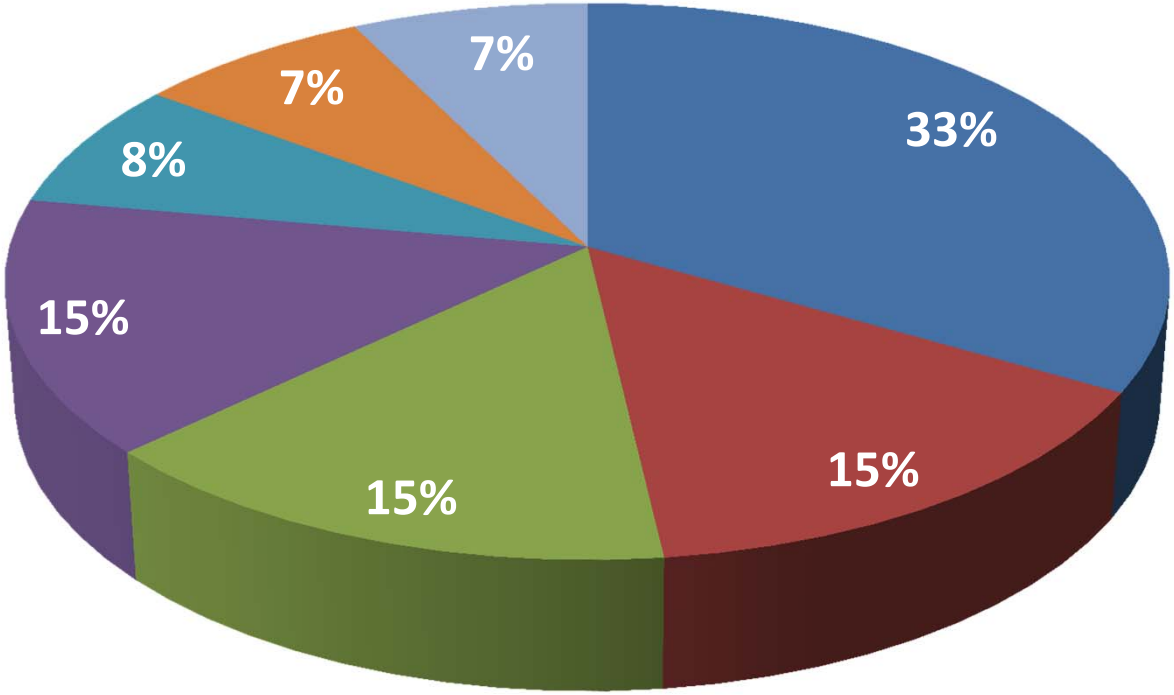


- 台灣
- 大陸
- 日韓
- 美國
- 歐洲

2018年前三季銷售分析-產品別



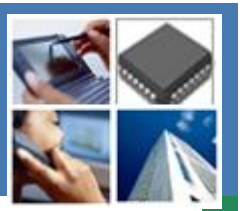
2018年前三季銷售分析-應用別



- IoT
- Storage
- Artificial Intelligence
- Others
- Audio/Video
- Navigation
- Networking

*Based on agreement numbers

2018年前三季簽約客戶分析



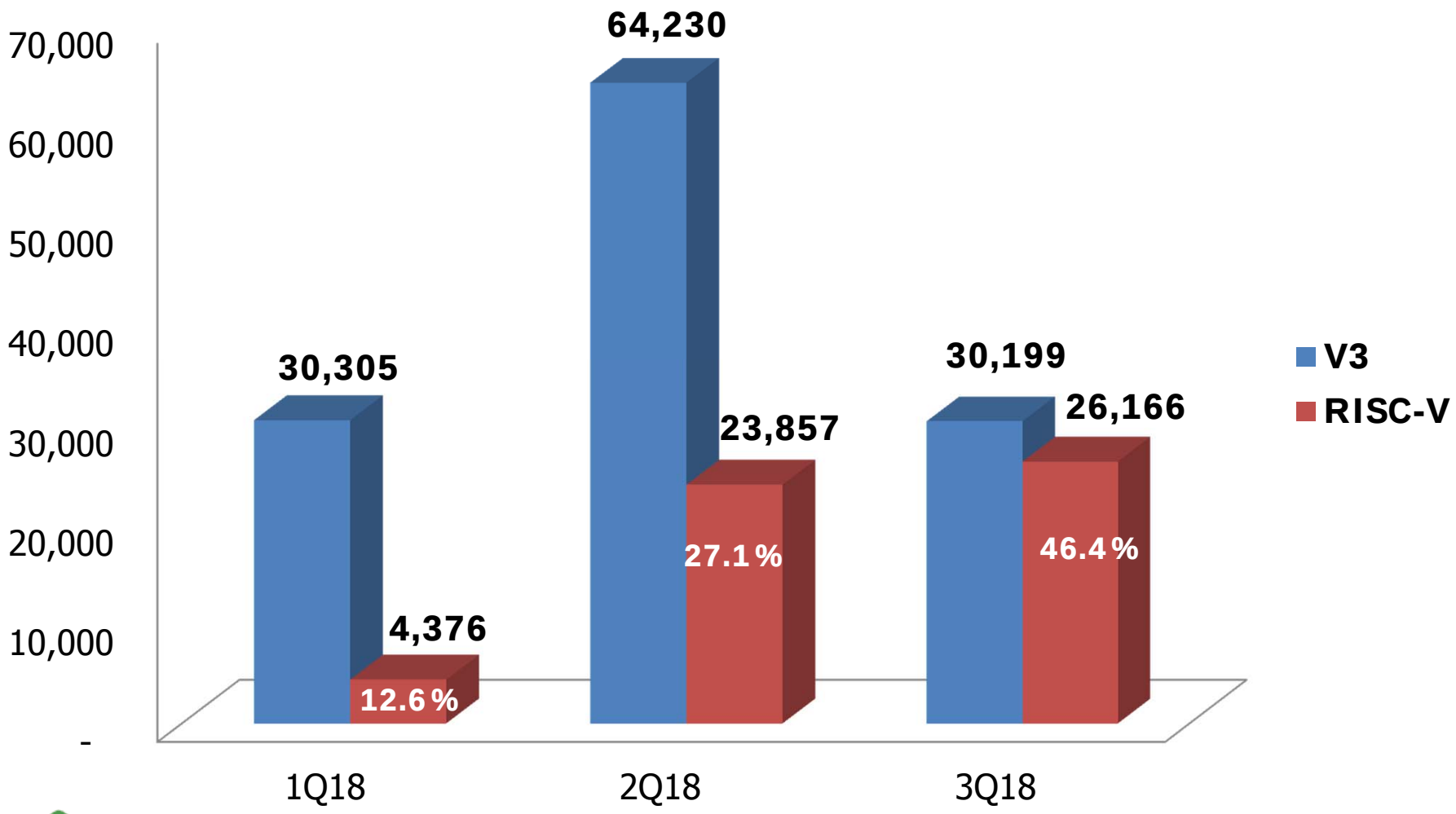
◆ Agreements signed for Q3: 6, total YT3Q18: 27

Andes Core	3Q18	YT3Q18	簽約客戶數統計
N7, N8, N9	Mainland x 1 (車用wiFi)	Mainland x 5, US x 2, Korea x 3, Taiwan x 1	11
N10, D10, N13,N15	Japan x 1 (FPGA)	Mainland x 4, US x 1, Taiwan x 1, Japan x 1	7
D15		Europe x 1	1
N25, NX25, AX25	Mainland x 1 (SSD), Japan x 1 (Storage), Taiwan x 2 (AI, Finger print)	Mainland x 3, US x 1, Taiwan x 3 , Japan x 1	8

RISC-V

2018年前三季銷售分析-RISC-V

(單位:新台幣千元)



產品應用

豐富多樣的客戶應用

Consumer

- Touch Screen
- eBook / eDictionary
- Power management
- Bio-medical device
- CMMB
- MCU
- TCON

Storage & Sensor

- USB3.0
- SSD, eMMC
- Anti-virus
- Sensor Hub
- mSATA
- Secure SD
- Fingerprint Recognition

Communication & IoT

- Wireless display
- WiFi, Bluetooth
- GPS, GPON, NFC
- Gateway / router
- Portable Karaoke
- Sigfox LPWAN
- IoT Cat0 base station
- IoT MCU
- ESL
- Smart Meter
- Smart Lighting

Industrial & Video

- Motor Control
- Wireless Charger
- Surveillance
- Barcode scanner
- ADAS
- VEDR
- 4K2K CODEC
- 8K4K CODEC

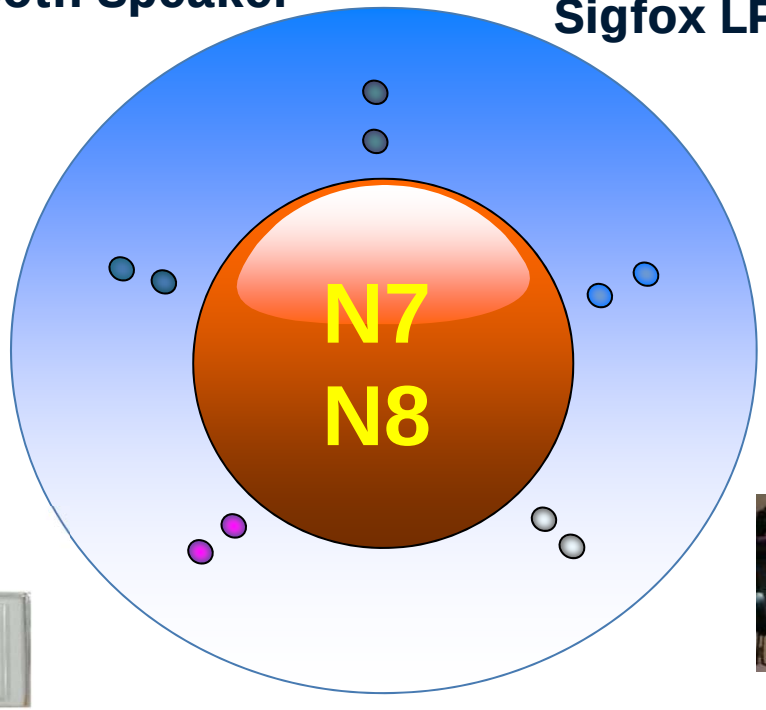
and more…..

物聯網應用 - 1

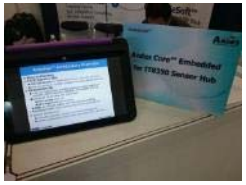
Bluetooth Speaker

Sigfox LPWAN

Healthcare device



Wearable device



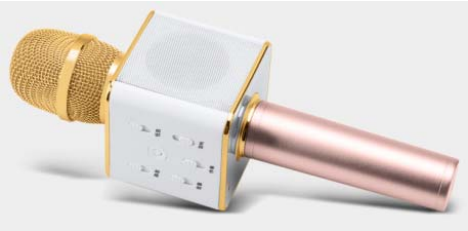
Sensor Hub

Electronic price tags

物聯網應用 - 2

Wearable devices

Drone



Portable Karaoke

N9
D10

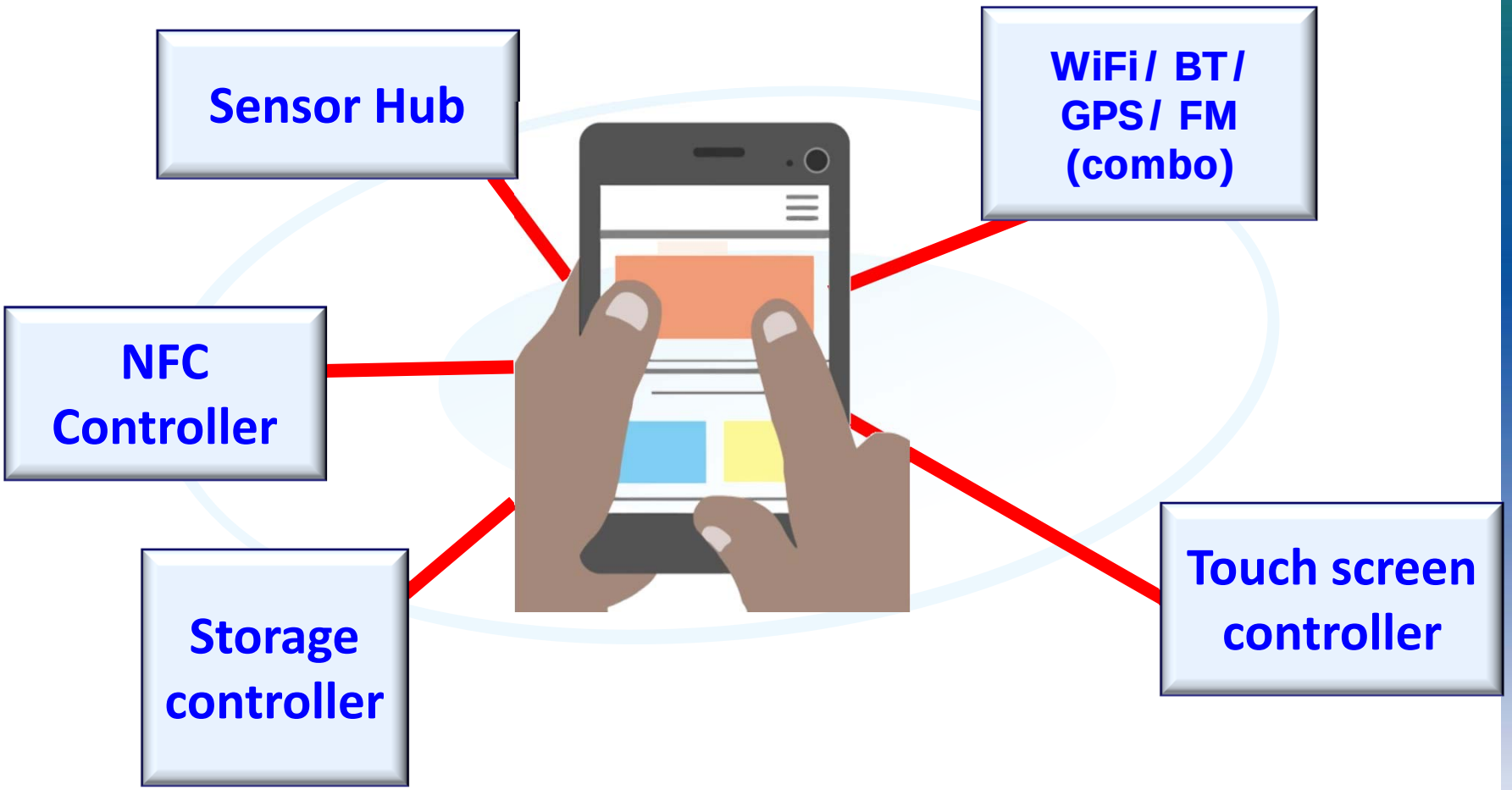
WiFi / GPS / FM / Bluetooth combo

GPS / Beido in shared bikes

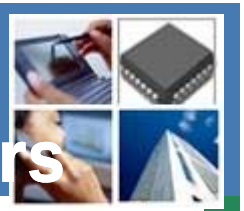
Contactless payment (NFC)

晶心嵌入智能手機

1 in 5 Smart Phones are with Andes Embedded worldwide



Andes Embedded
in Consumer Devices, Cars and Datacenters



Switch:
MXIC Flash Ctlr

Echo Dot2:
Mediatek WiFi IoT

Bike Sharing:
GPS Ctrl

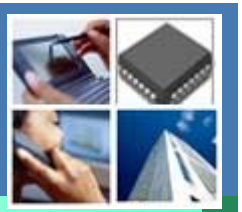
X-Trail:
ADAS Ctlr

- In leading machine learning computers for datacenter
- In tier-one switch routers for datacenter

- Recent applications: Set-top Boxes, 802.11ax, machine learning processors (using Andes Custom Extension, ACE)

新產品及生態系統

完整產品線



- 今年度的晶心嵌入式科技研討會推出晶心A系列微處理器核心

A N D E S

RISC-V

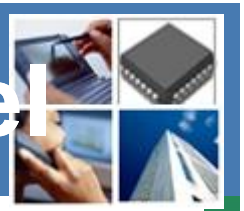
V5 AndesCore™ Processors

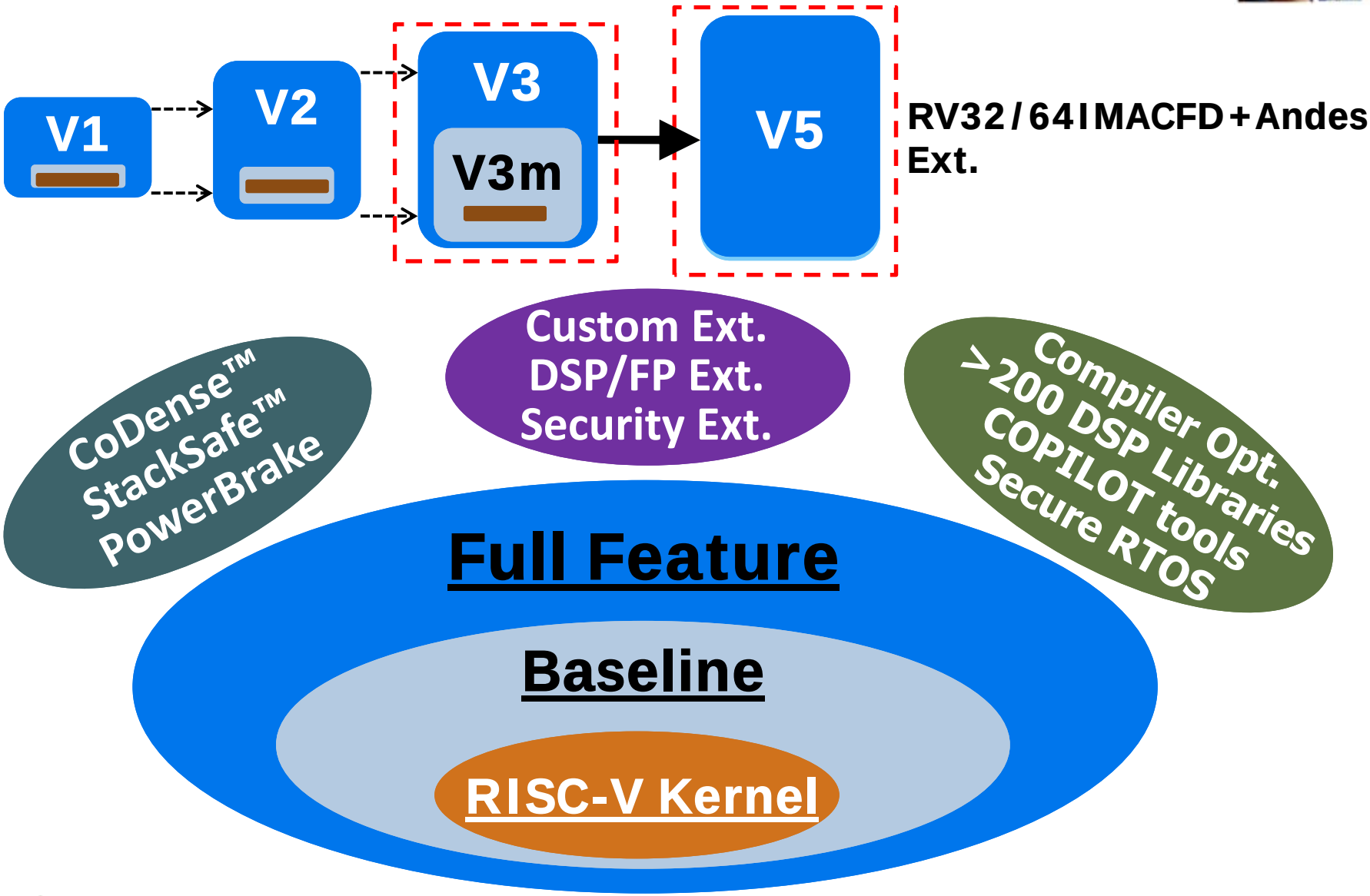
N25/NX25

N25F/NX25F

A25/AX25

AndeStar™ V5:新一代的 ISA Kernel





AndesCore™ V5 Families

Leading Performance

StackSafe™

CoDense™

PowerBrake

Next Gen.
V5 ISA,
Advanced Micro-Architecture

Virtual Memory Support

A25
V5, 32-bit
5-stage, 1GHz
MMU, FPU,
ACE...

AX25
V5, 64-bit
5-stage, 1GHz
MMU, FPU,
ACE...

I/D Local Memories

I/D Caches

Branch Prediction

Modern Architecture

N25(F)
V5, 32-bit
5-stage, 1GHz
PMP, FPU,
ACE...

NX25(F)
V5, 64-bit
5-stage, 1GHz
PMP, FPU,
ACE...

ACE

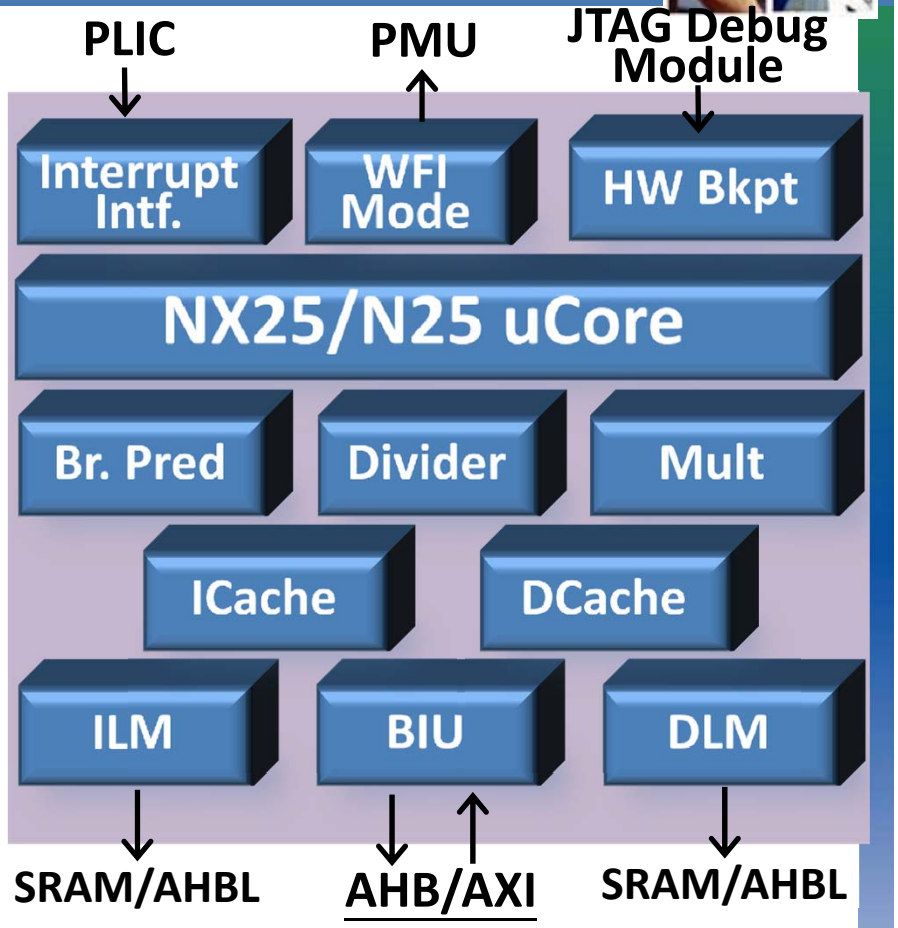
64-bit AXI/AHB

ECC

◆ 28HPC RVT, SS, 0.81V, 0C, with I/O constraints.

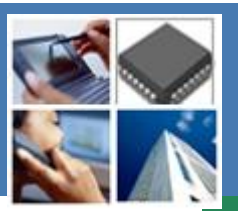
V5 AndesCores: 25-系列 Baseline

- **N25: 32-bit, NX25: 64-bit**
  - From scratch for the best PPA
  - Very configurable
- **AndeStar V5 ISA**
- **5-stage pipeline**
- **Configurable multiplier**
- **Optional branch prediction**
- **Flexible memory subsystem**
  - I/D Local Memory (LM): to 16MB
  - I/D caches: up to 64KB, 4-way
  - Optional parity or ECC
  - Hit-under-miss caches
  - load/store: unaligned accesses

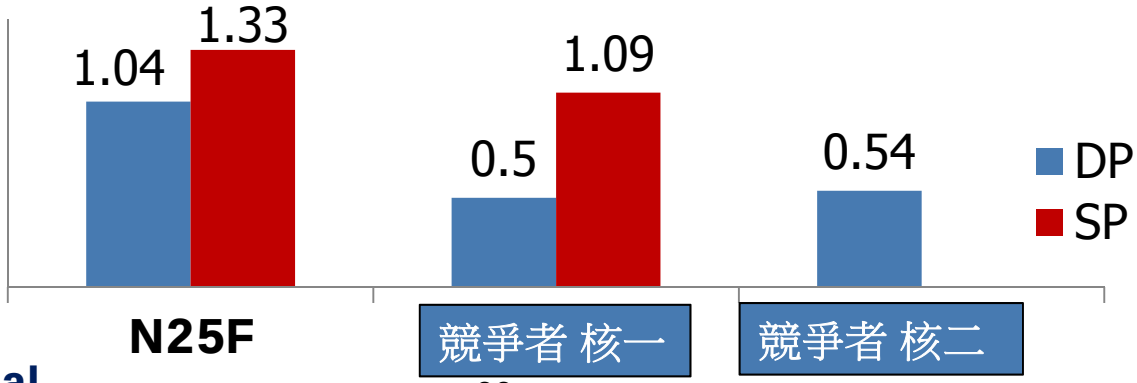


- **N25 sample configurations @TSMC 28HPC+ RVT:**
  - Small config: 37K gates, 1.0 GHz (worst case)
  - Large config: 130K gates, 1.2GHz (worst case)
  - **Best-in-class Coremark: 3.58/MHz**

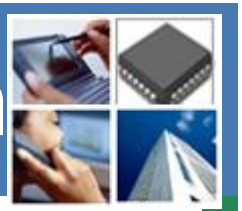
V5 AndesCores: New 25-系列



- **N25/NX25:**
  - Fast-n-small for control tasks in AR/VR, networking, storage, AI
- **N25F/NX25F: +FPU**
  - +, –, x, x+, x–: pipelined 4 cycles
  - ÷, √ : run in the background
    - ◆15 for SP, 29 for DP
  - FP load/store: support HP
- **A25/AX25: +FP +Linux**
  - Support RISC-V MMU and S-mode
  - 4 or 8-entry ITLB and DTLB
  - 4-way 32~128-entry Shared-TLB
- **Whetstone/MHz:**



ACE: Andes Custom Extension



Verilog user.v

concise RTL

semantics, operands, test-case spec

script user.ace

COPILOT

Custom-OPtimized Instruction deveLOpment Tools

Extended Tools + **Compiler Asm / Disasm Debugger IDE**

Extended ISS + **CPU ISS (near-cycle accurate)**

Extended RTL + **CPU RTL**

Extensible Baseline Components

Automated Env. For Cross Checking

Test Case Generator

Extended RTL

Extended ISS

Executable or library

Source file

積極參與RISC-V社群活動

Foundation Working Groups (partial list)

Bit Manipulation
AMD, Andes Technology, BAE Systems, Esperanto Technologies, ETH zürich, lowRISC, MediaTek, Microsemi, SiFive, Syntacore

Compliance
codasip, BAE Systems, bluespec, Microsemi, NVIDIA, SiFive, Syntacore, Berkeley Architecture Research

Debug
SiFive, Andes Technology, BAE Systems, bluespec, cortus, Google, NVIDIA, lowRISC, RA Logic, Syntacore, Verisilicon, ultraSoC

Memory Model
NVIDIA, IBM, Princeton University, Verisilicon, lowRISC, MIT CSAIL, SiFive, Andes Technology, bluespec, BAE Systems, Western Digital, Syntacore

Privileged Spec
SiFive, Andes Technology, BAE Systems, Esperanto Technologies, bluespec, NVIDIA, Western Digital, lowRISC, Syntacore, Berkeley Architecture Research, MIT CSAIL

Vector
SiFive, Andes Technology, NVIDIA, Micron, Google, lowRISC, MediaTek, Microsemi, Esperanto Technologies, Syntacore, Berkeley Architecture Research, ETH zürich, Western Digital, BAE Systems

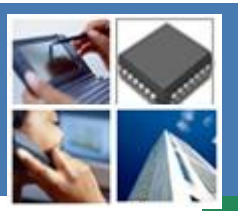
Security
NVIDIA, MediaTek, Microsemi, Huawei, Blockstream, SiFive, Esperanto Technologies, BAE Systems, Andes Technology, DRAPER, ultraSoC, AMD, NXP

Base ISA/Opcode
SiFive, Andes Technology, Esperanto Technologies, Western Digital, Syntacore, lowRISC, Berkeley Architecture Research, BAE Systems

Andes在RISC-V硬體基礎設施上的貢獻

- **Contributing architecture extensions too**
  - Chair of the P-ext (Packed SIMD/DSP) Task Group
  - Co-chair of Fast Interrupt Task Group
  - Closely reviewing activities of other Task Groups

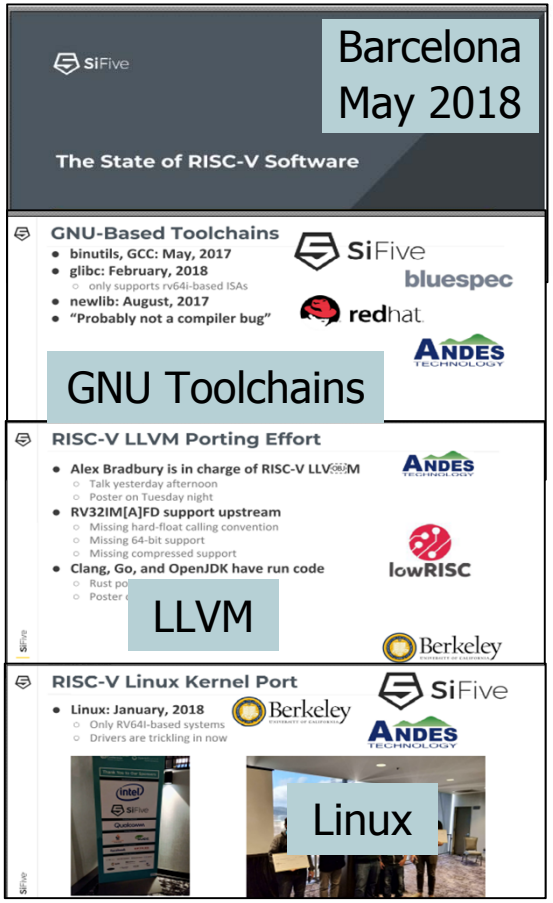
Andes協助強化RISC-V生態系統



- More choices for customers are good
- Andes works closely with partners to grow RISC-V ecosystem

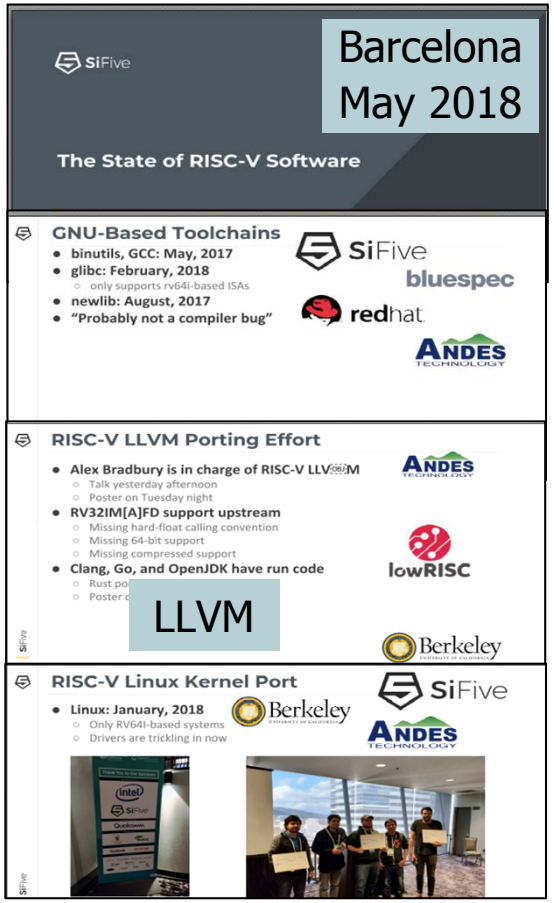
RISC-V軟體生態系統: GNU Toolchain

- **GCC, binutils**: May, 2017
- **Newlib**: Aug, 2017
- **Glibc (rv64i)**: Feb, 2018
- **GDB**: Mar, 2018
- **OpenOCD**: July, 2018
- **Glibc (rv32i)**:
  - Submitted in July 2018 (by Andes)
  - Review in progress



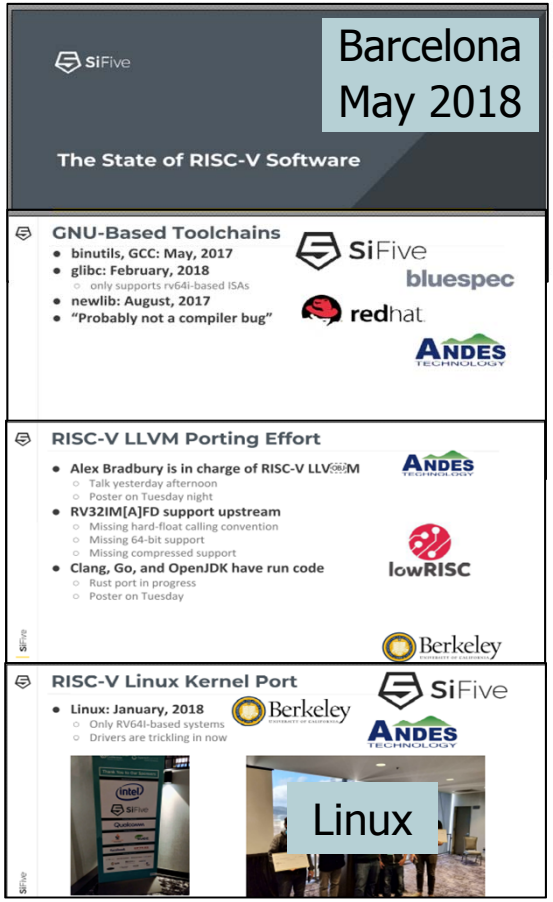
RISC-V軟體生態系統: LLVM Compilation

- **LLVM**:
  - RV32IMAFDC: June, 2018
  - Relaxation: May, 2018 (by Andes)
  - 64b support: review in progress since Oct, 2018
  - Missing hard-float calling convention
- **compiler-rt**: Mar, 2018
- **LLD**: Aug, 2018 (by Andes)
  - Initial port (relocation and TLS) in Oct. 2017
  - Dynamic linking review in progress since Oct, 2017
  - Missing link-time relaxation

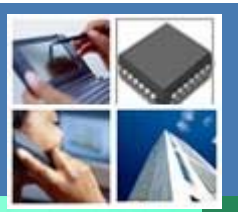


RISC-V軟體生態系統: Linux

- **U-boot**: Jan, 2018 (by Andes)
- **Kernel (rv64i)**: Jan, 2018
- **Key utilities**: (by Andes)
  - Perf: Feb, 2018
  - Kernel Module: May, 2018
  - Ftrace: May, 2018
- **Kernel (rv32i)**: Jun, 2018 (by Andes)
- **Kernel with no FPU**: Oct, 2018



Andes在RISC-V上重要的定位



Complete product portfolio

Reliable RISC-V core IP provider

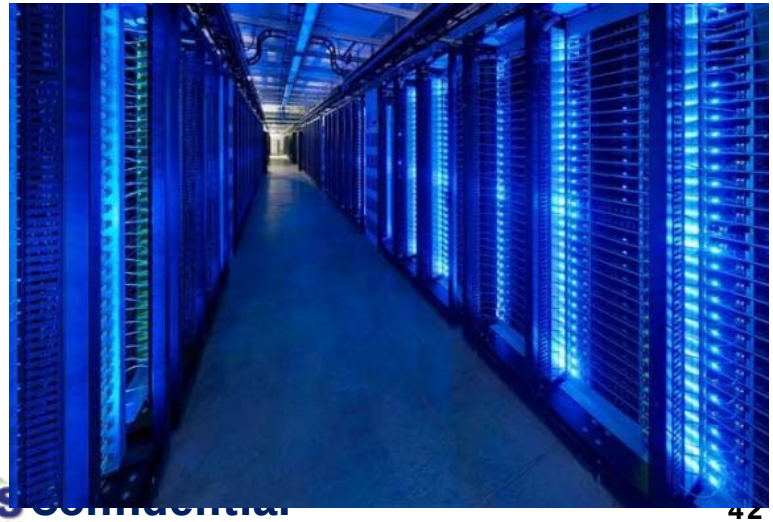
RISC-V cores that run Linux

Extreme low power consumption, high computing efficiency

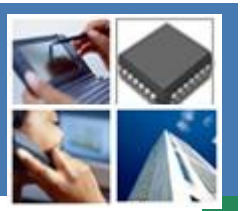
World's Leading Customer-Extension Capable RISC-V Core

截至目前RISC-V Design Win

- **Ten design win for Andes RISC-V Core IPS:**
  - **NX25: Enterprise SSD (Taiwan)**
  - **N25: AI (China – with ACE), Blockchain (China), HD-PLC (Japan), SSD (China), Fingerprint (Taiwan), AI (Taiwan), Research/Academic (Taiwan)**
  - **N25/AX25: FPGA for AI (US)**
  - **AX25: FPGA for AI (China)**
- **Eleven design service providers joined Andes RISC-V Easy Start Program:**
  - **US x 3, Europe x1, Korea x 1, China x 2, Taiwan x 4**



AndesCore™ 競爭優勢



AndesCore™	AndesCore / Competitor Power Efficiency[1] (DMIPS/mW)	Competitors
N7	+42%	Cortex-M0+
N8	+43%	Cortex-M3
N9	+43%	Cortex-M3
D10	+48%	Cortex-M4
N13	+185%	Cortex-A5
N13	+45%	Cortex-R4
D15F	+121%	Cortex-M7

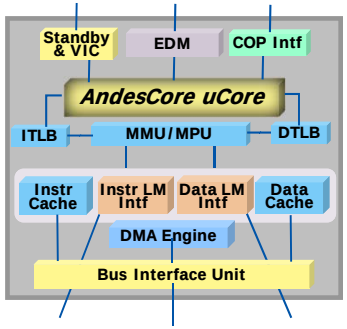
1. Power Efficiency is DMIPS/MHz divided by power consumption (mW/MHz) when running Dhrystone.

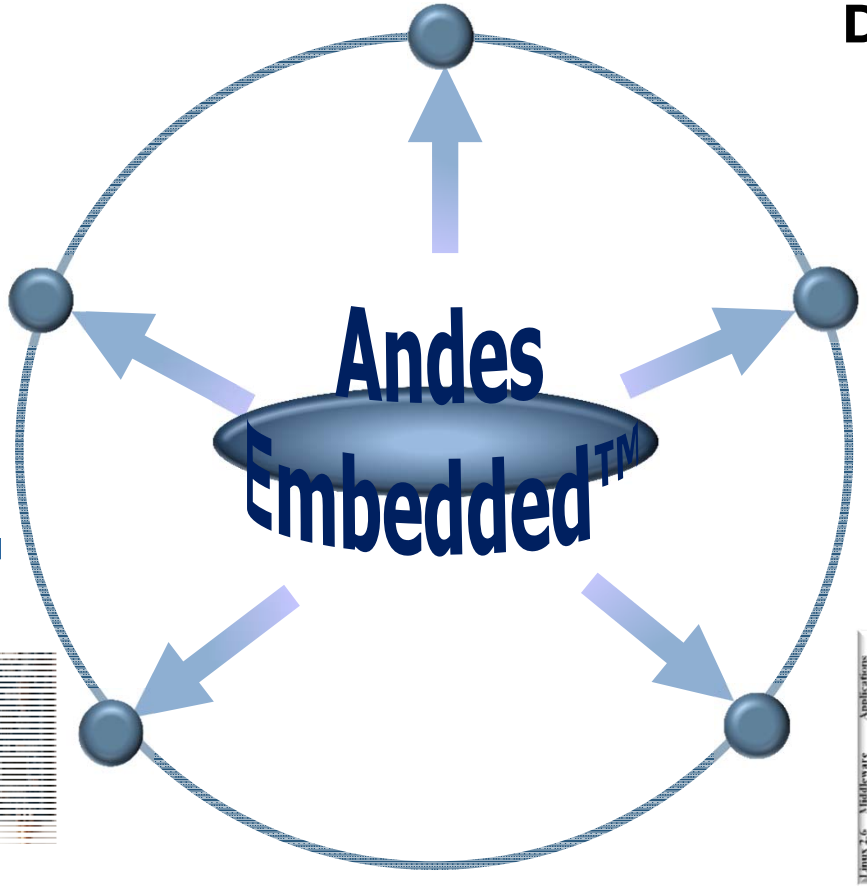
64位元架構及生態系統

Processor Architecture
AndeStar™ V5

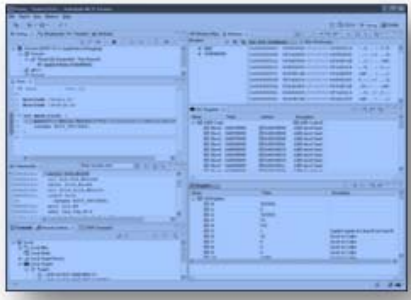
```
smw.adm  $r1,[$sp],$r5,0x0
smw.adm  $sp,[$sp],$sp,0x2
addi     $sp,$sp,-8
sethi    $r1,0x50a
lwi      $r1,[$r1+#0x98]
mov55    $r2,$r0
mov55    $r0,$r1
lwi      $r1,[$r1+#0x8]
addi     $r3,$sp,12
```

Processor IP's
AndesCore™ NX25

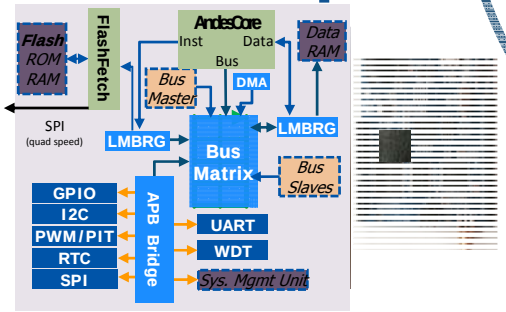




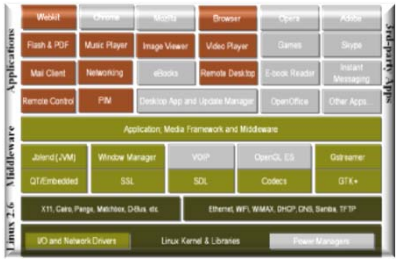
Development Tools
AndeSight™



Development Platforms
AndeShape™



SW Stacks
AndeSoft™



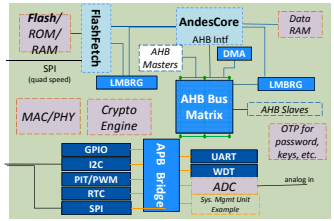
生態系統: Andes 與 Knect.me

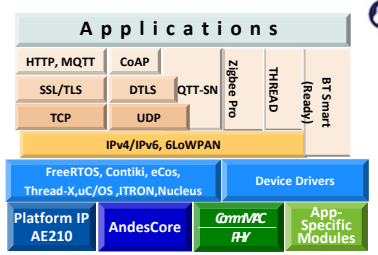
ANDES TECHNOLOGY

knectme™

Knect.me 生態系統

- **Built up Ecosystem *knect.me* to help IoT Developing**
  - to **knect** solutions - Silicon IP's, SW stacks, tools, applications, systems and products
- **Includes:**
  - SoC IP Platforms
  - Software Stack
  - Development Boards
  - Development Tools
- **To Form a IoT League**
  - to **knect** chip vendors, partners, application developers, system vendors





knectme™

近期獲獎

ANDES TECHNOLOGY

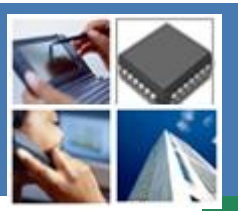
引領新興科技潮流

- “2018 Top25最佳新興科技解決方案提供公司”

— CIO Advisor Magazine

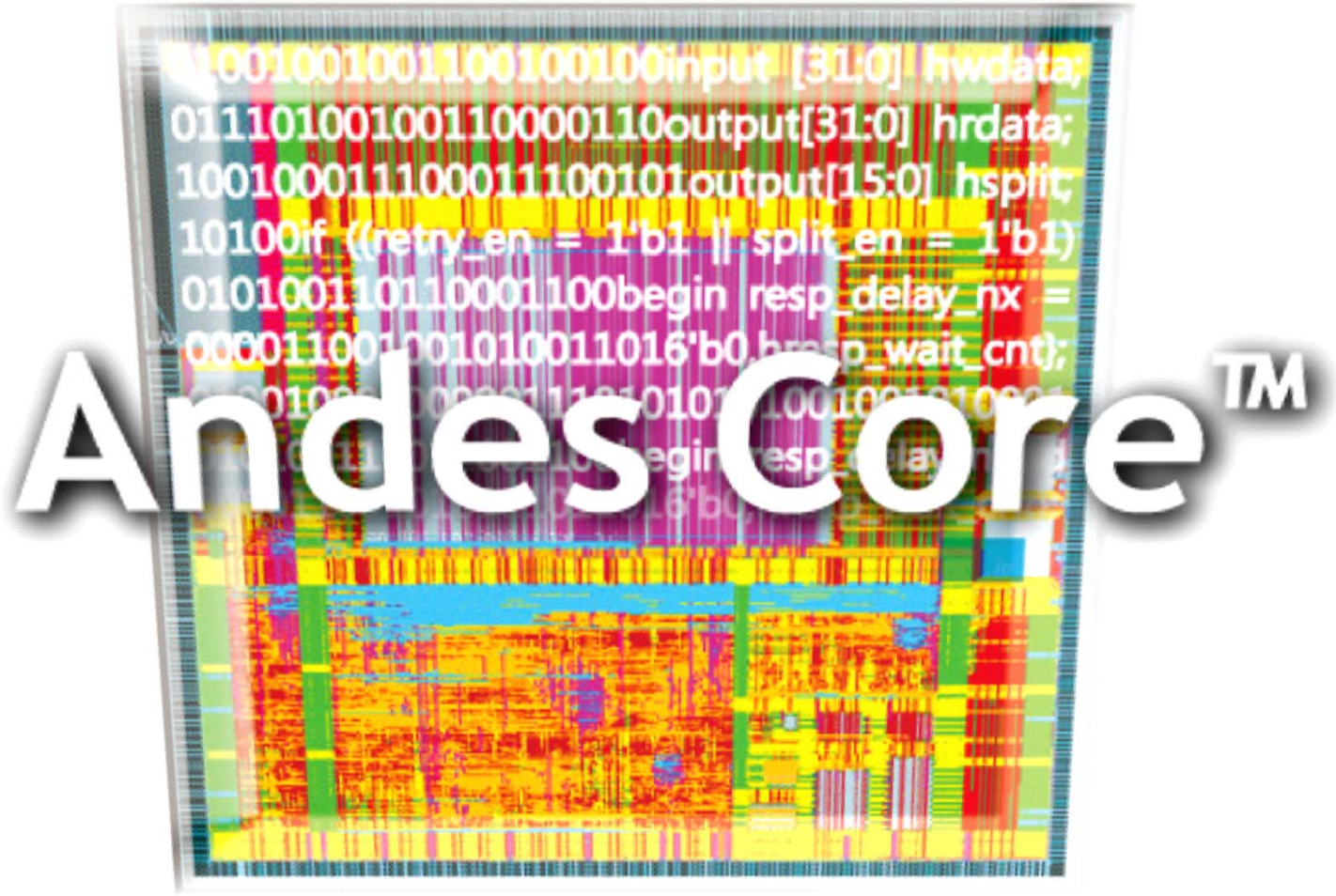
總結

晶心科技擴大產品陣線,強化生態系統



- 晶心科技積極參與 RISC-V 基金會科技與社群發展，與 RISC-V 生態系統互助，例如對GCC compiler、 LLVM compiler 、 fast interrupt 、 vector instructions等技術多所貢獻。晶心科技目前領導著RISC-V 基金會之DSP指令集工作小組，執行RISC-V P-Extension的規格發展全球性討論，朝向未來的 正式發表而努力中。
- 晶心科技已陸續與全球 11家Design service houses簽訂合約，授權其協助客戶開發內嵌 Andes RISC-V core的ASIC (稱為Andes RISC-V Easy Start Program)，創造晶心、Design service house與產業共贏的局面。此一行動仍在持續中，預期在數月內完成與全球二十家Design service houses簽訂 Andes RISC-V Easy Start Program 合約，形成 一個聯盟，強化 Andes RISC-V 生態系統。

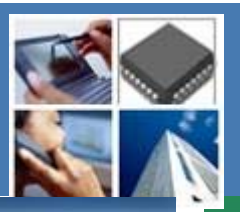
謝謝指教

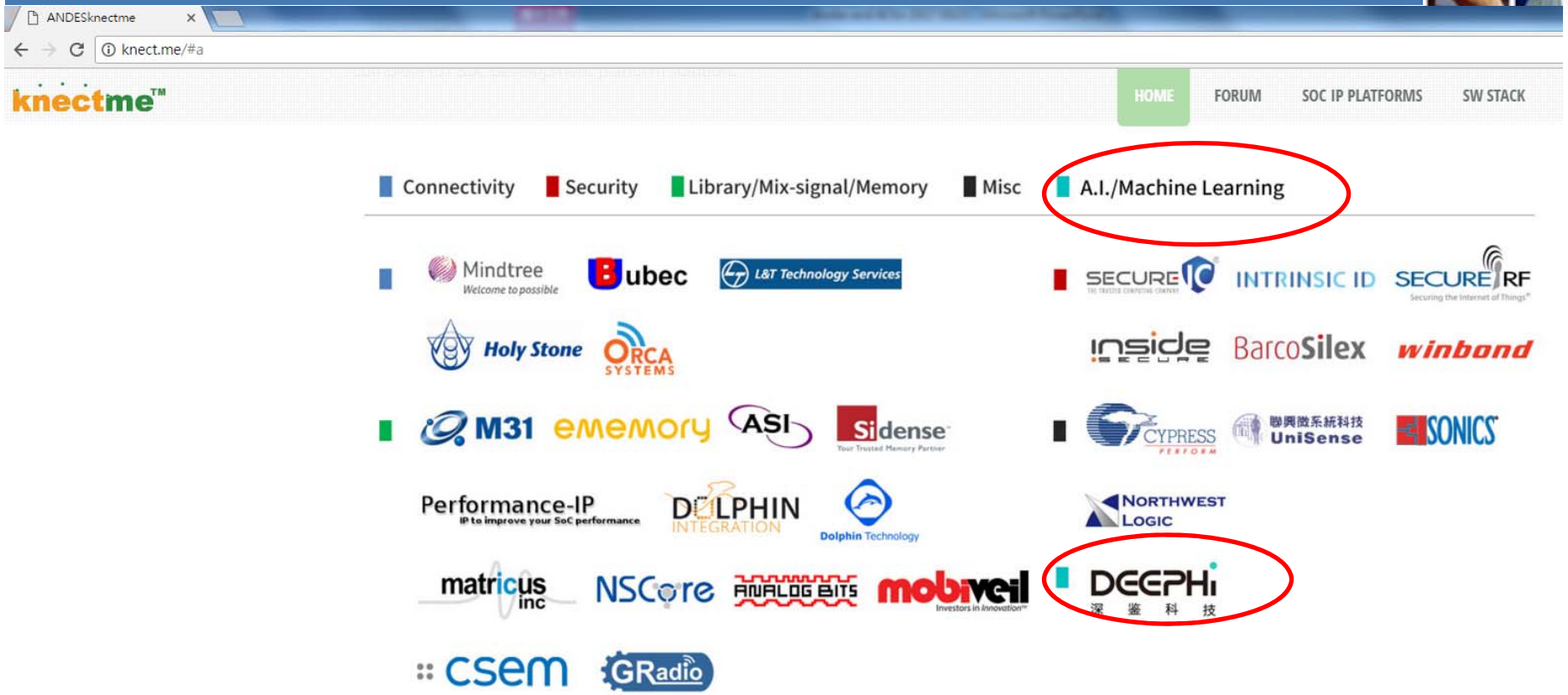


www.andestech.com

問與答

Added A.I. to Knect.me Ecosystem





What is "IoT League"? We invite Andes' customers to provide products information which contains AndesCore. IoT League can enhance exposure and reputation in IoT domain. Various applications can help Andes' customers to attract more and more users to adopt their IoT products.

Companies in alphabetical order

AIROHA HYCON HYCON TECHNOLOGY ITE ITE TECH.INC. M2Communication Weltrend Wave Computing.