Andes Technology Corporation
2018 Investor Conference Report

Driving Innovations™

Stock #: 6533
2019/03/26

Safe Harbor Notice

Except for the historical information contained herein, the matters addressed in this presentation are forward-looking statements that involve certain risks and uncertainties that could cause actual results to differ materially, including but not limited to weather, impact of competitive products and pricing, industry-wide shifts in the supply and demand for semiconductor products, rapid technology change, semiconductor industry cycle, and general economic conditions.

Except as required by law, Andes undertake no obligation to update any forward-looking statement, whether as a result of new information, future events or otherwise.

Agenda

- Overview of Andes Technology Corporation
- Operating Results
- Product Applications
- New Products and Ecosystems
- Andes Awarded
- Concluding Remarks

Overview of Andes Technology Corporation

Andes Highlights

- Founded in March 2005 in Hsinchu Science Park, Taiwan, ROC.
- Core RD team from **AMD**, **DEC**, **Intel**, **MIPS**, **nVidia**, and **Sun** veterans.
- Over 160 people now; 80% are engineers.
- EETimes' Silicon 60 **Hot Startups to Watch** (2012)
- **TSMC OIP Award** "Partner of the Year" for New IP (2015)
- A founding member of **RISC-V Foundation** (2016)
- **IPO in Taiwan Stock Exchange** (March 2017)

Andes Mission

- Innovate **performance-efficient** processor solution for **low-power** SoC

Emerging Opportunities

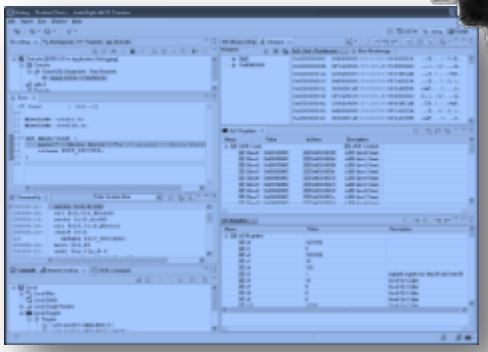
- **Smart** and **Green** electronic devices
- **Cloud Computing, Artificial Intelligence** and **Internet of Things**

Operating Results

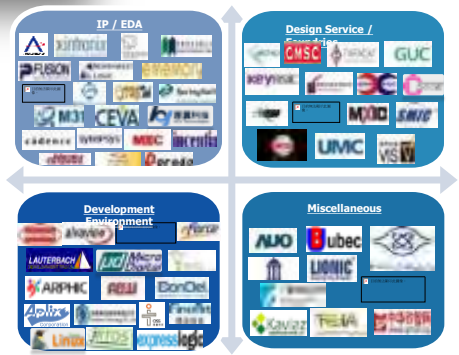
Business Status Overview

- **>160** commercial licensees
  - Geographically distributed in Taiwan, China, Korea, Japan, Europe, and USA.
  - **>246** license agreements signed

- AndeSight™ IDE:
  - >**14,000** installations

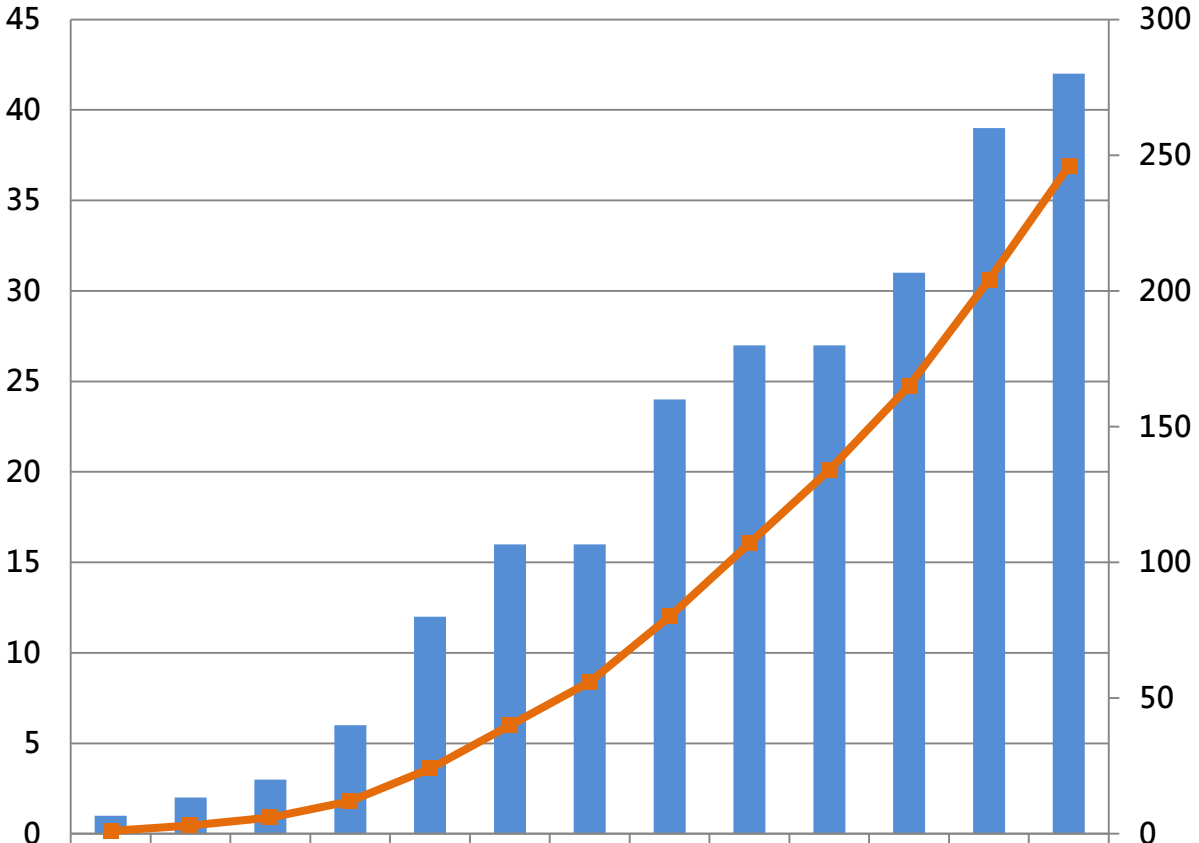


- Eco-system:
  - >**130** partners



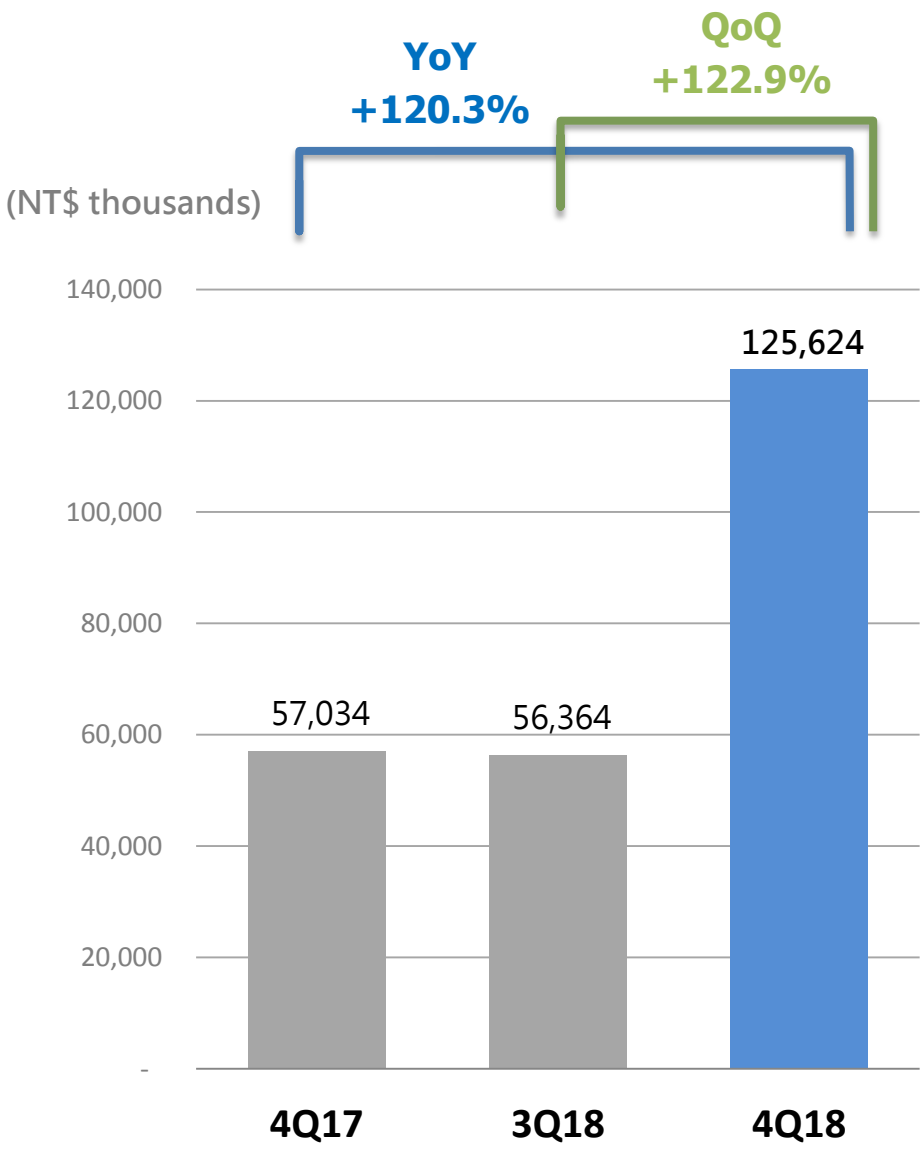
- **>3.6B** Accumulative SoC Shipped by the end of 2018

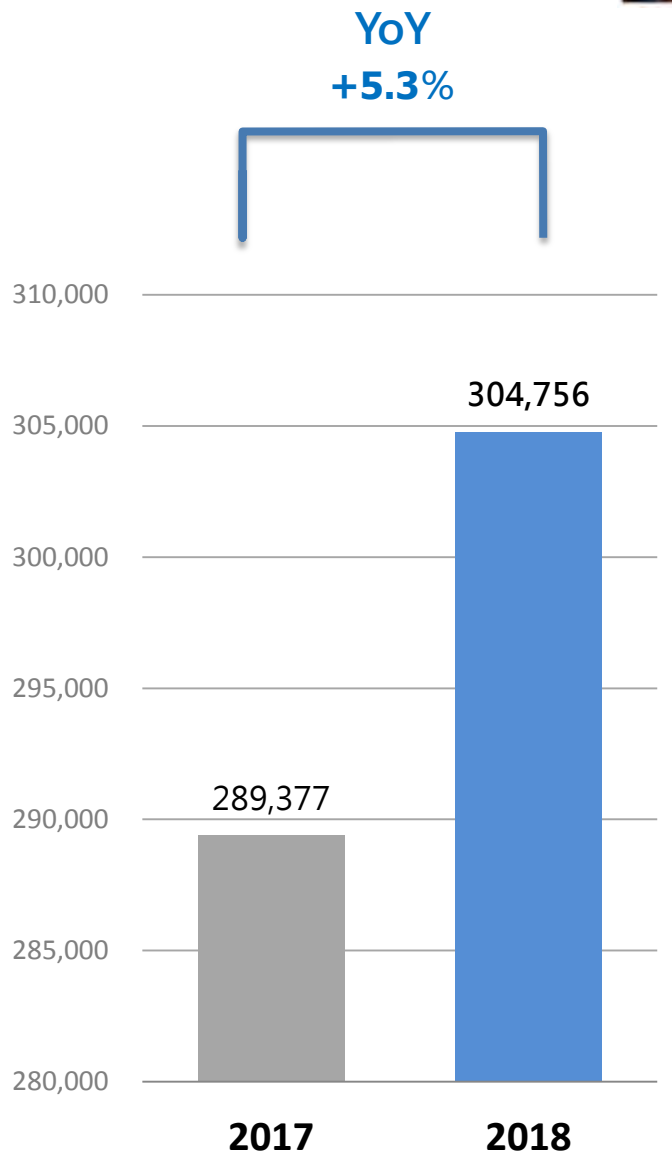
Agreement Growth Analysis



	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018
IP agreements	1	2	3	6	12	16	16	24	27	27	31	39	42
Accumulated IP agreements	1	3	6	12	24	40	56	80	107	134	165	204	246

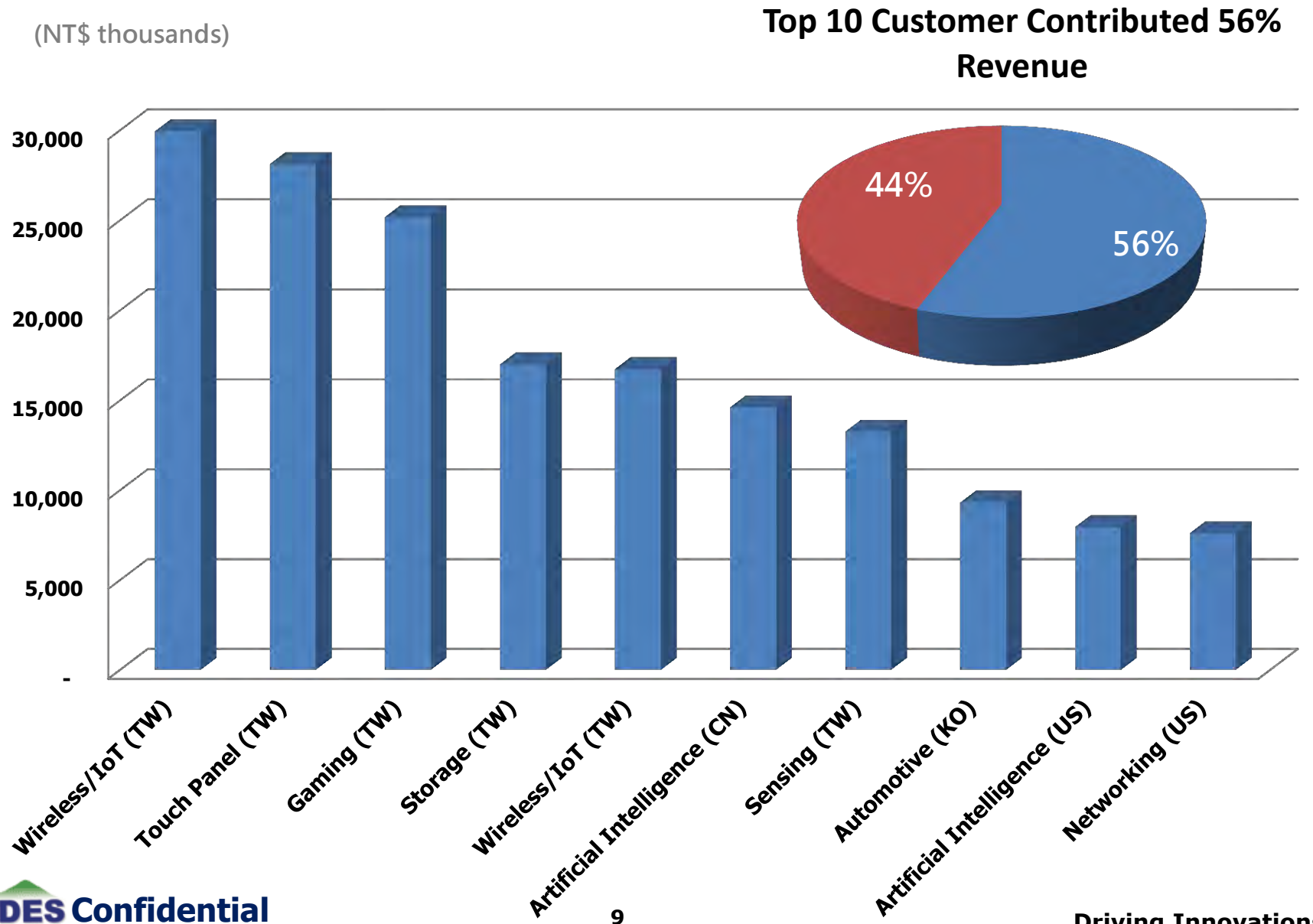
2018 Revenue Analysis



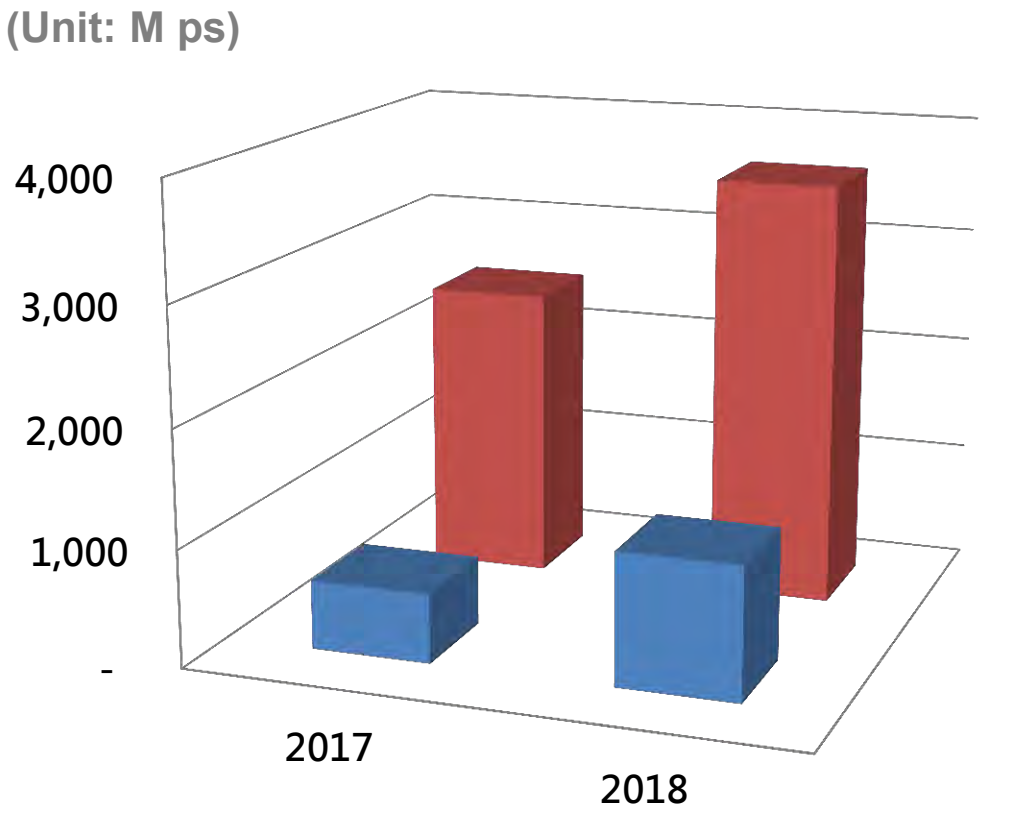


2018 Top 10 Customers Analysis by Revenue

(NT$ thousands)

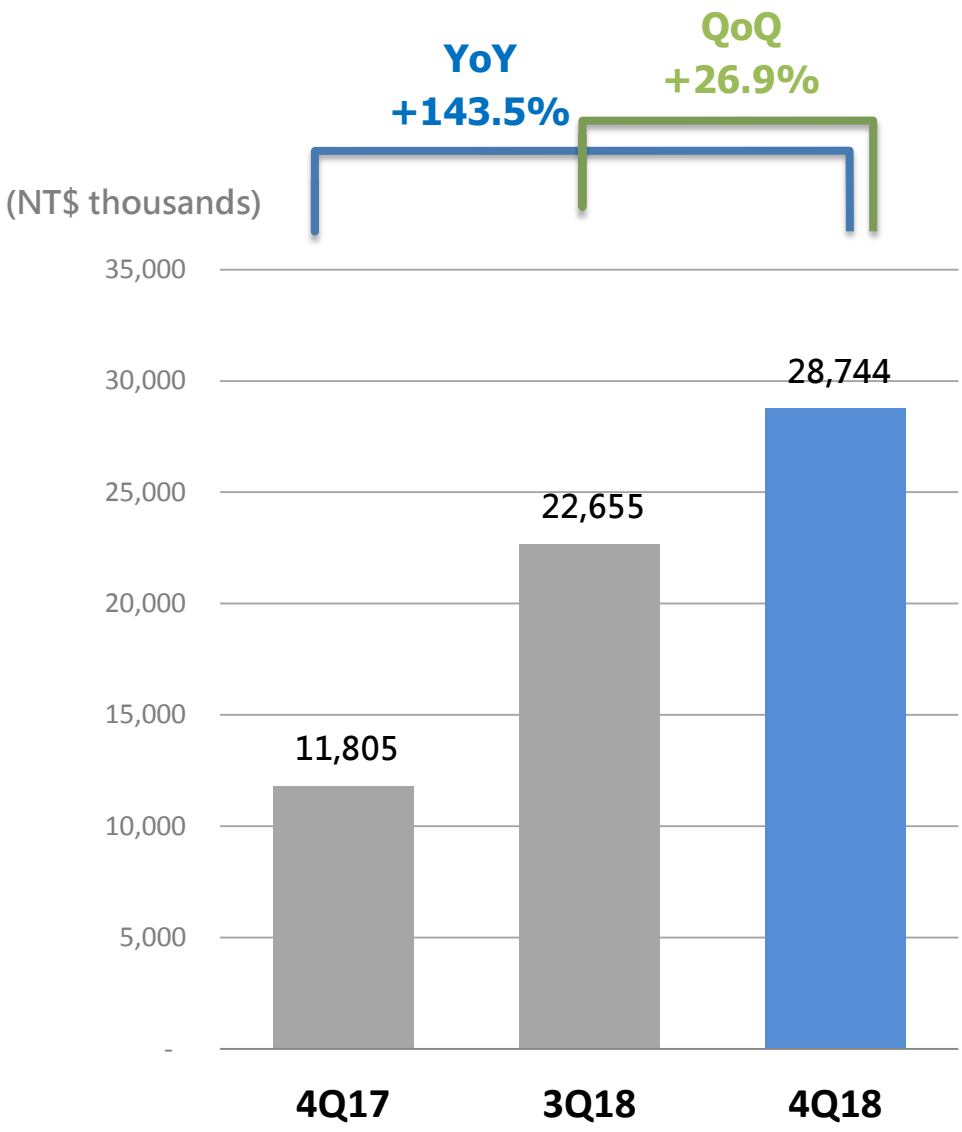


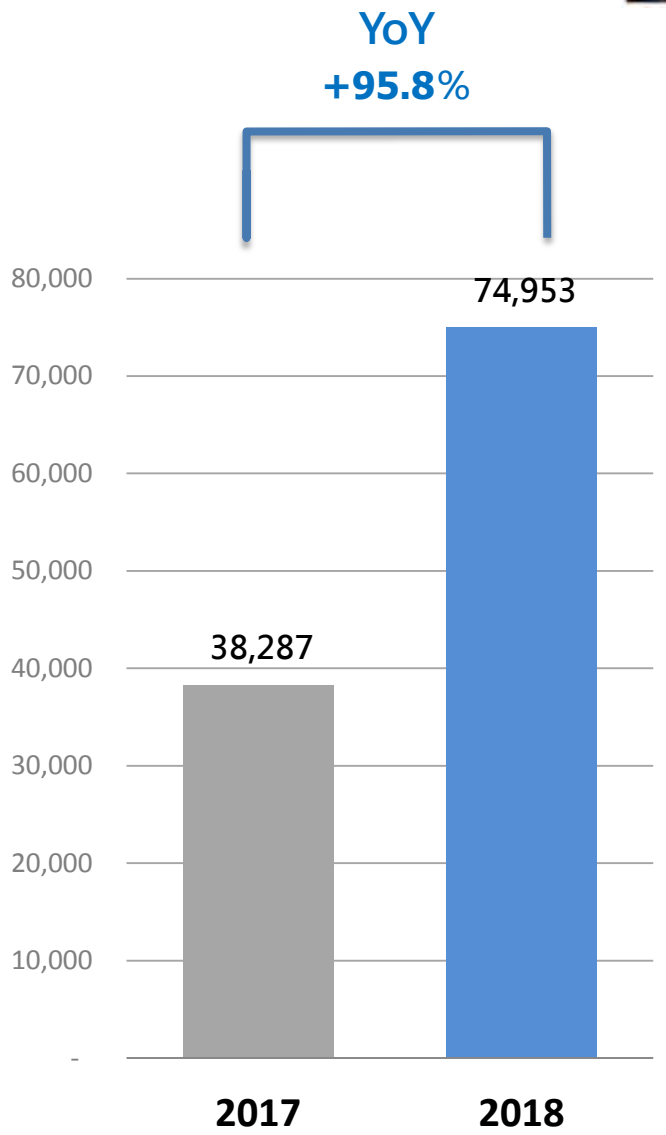
Total Customers Annual and Accumulated Shipment



	2017	2018
Annual Shipment	590	1,132
Accumulated Shipment	2,500	3,632

2018 Royalty Analysis

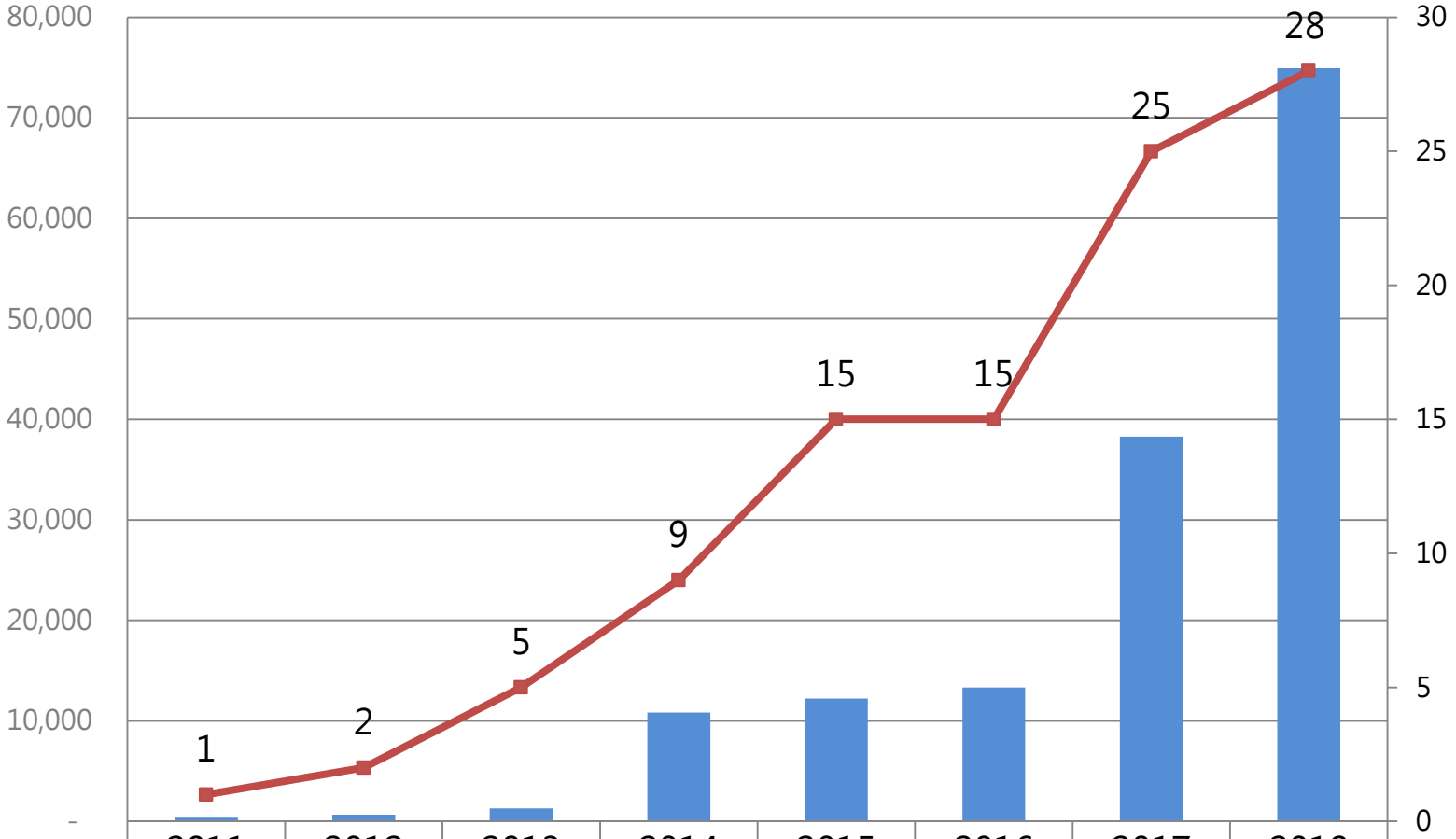




Royalty & Contributors Analysis

(NT$ thousands)

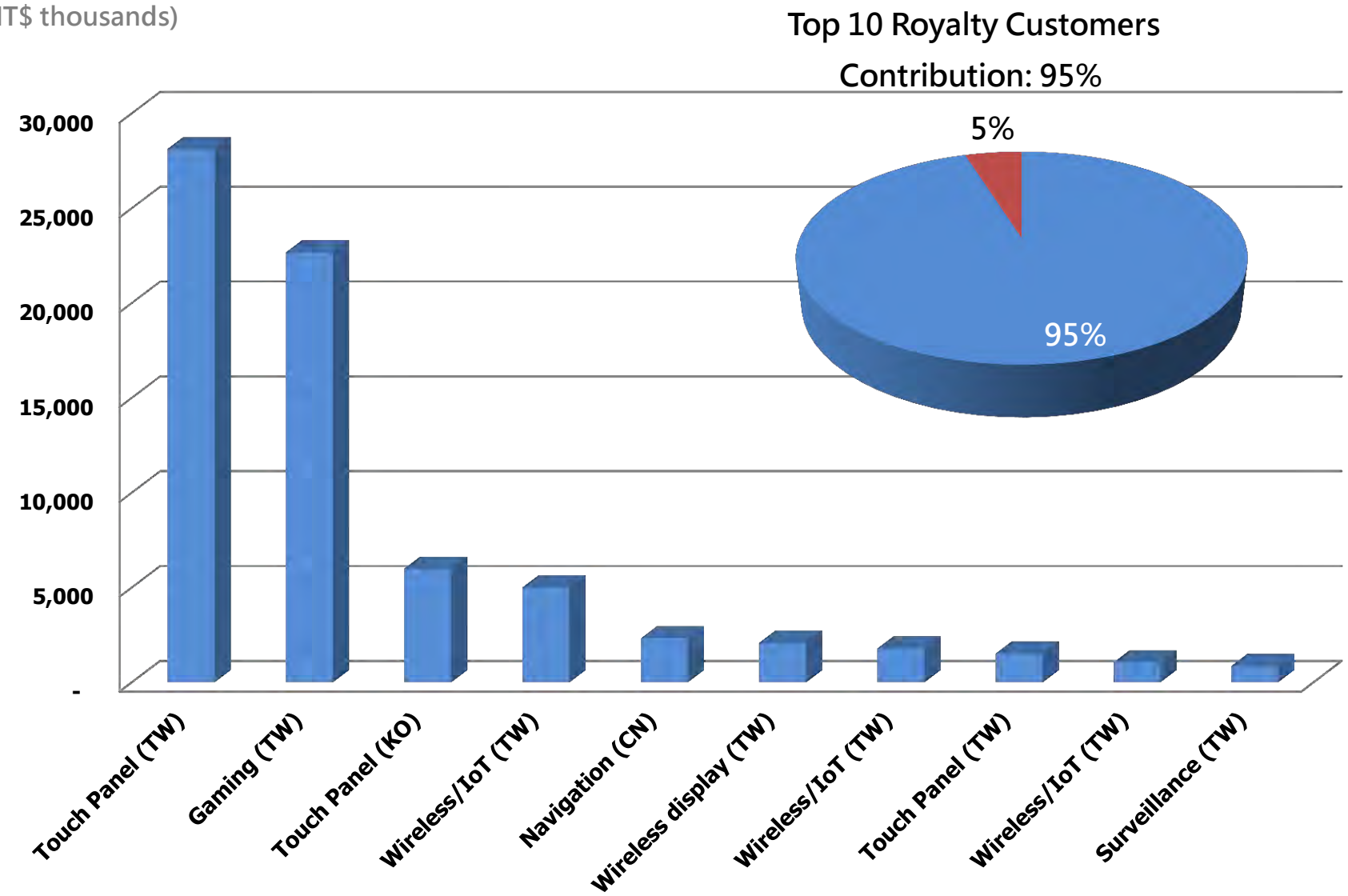
(Customer numbers)



	2011	2012	2013	2014	2015	2016	2017	2018
Royalty	445	660	1,285	10,819	12,232	13,320	38,287	74,953
Customer numbers	1	2	5	9	15	15	25	28

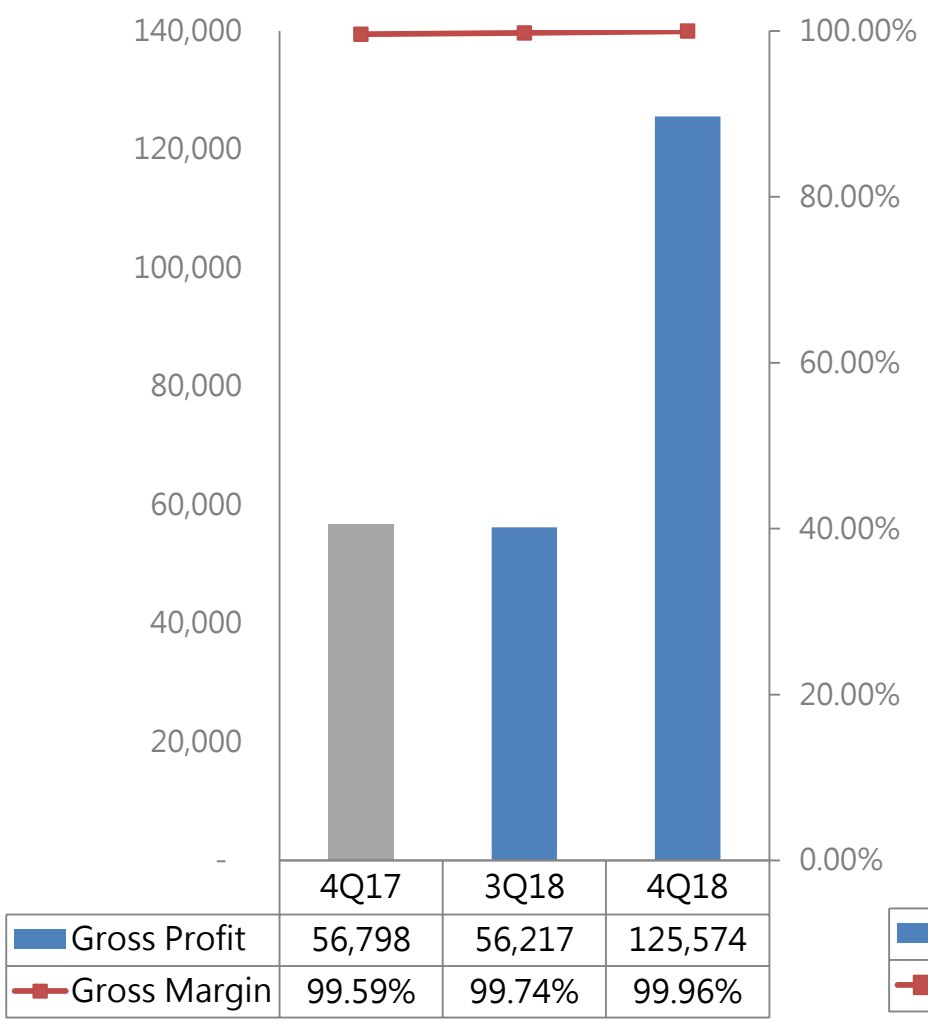
2018 Top Ten Royalty Contributors Analysis by Application

(NT$ thousands)

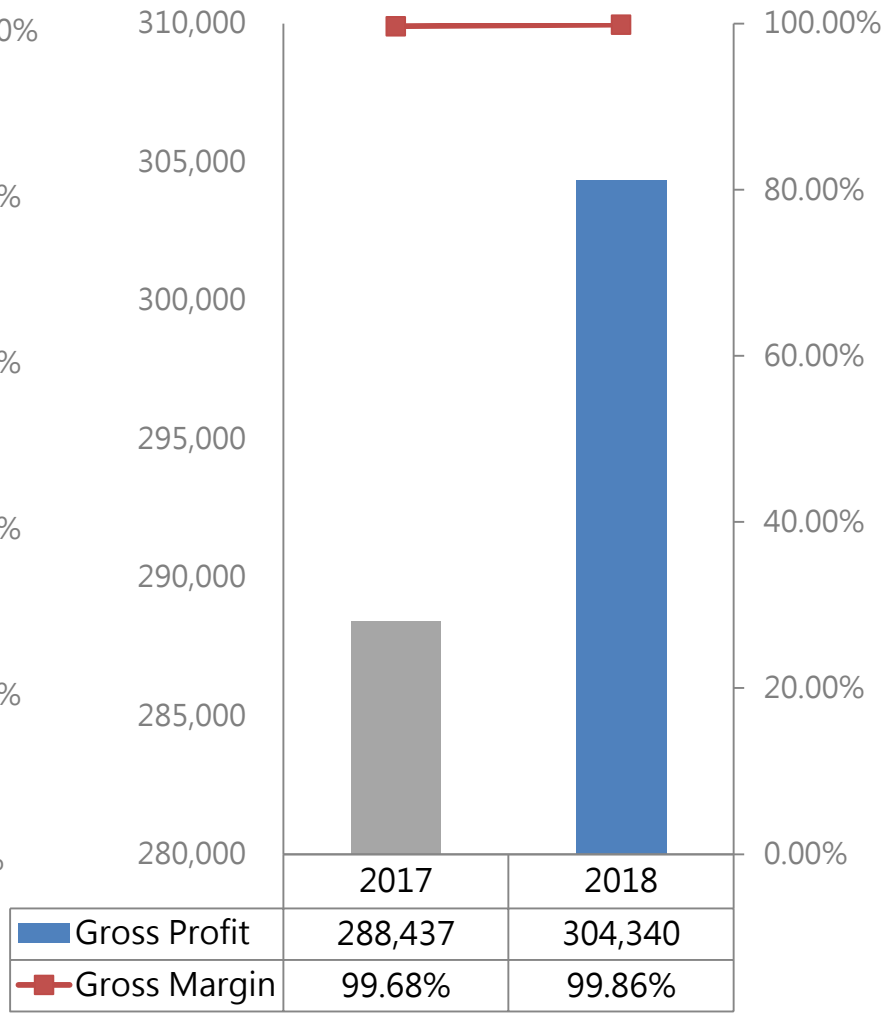


Consolidated Gross Margin

(NT$ thousands)

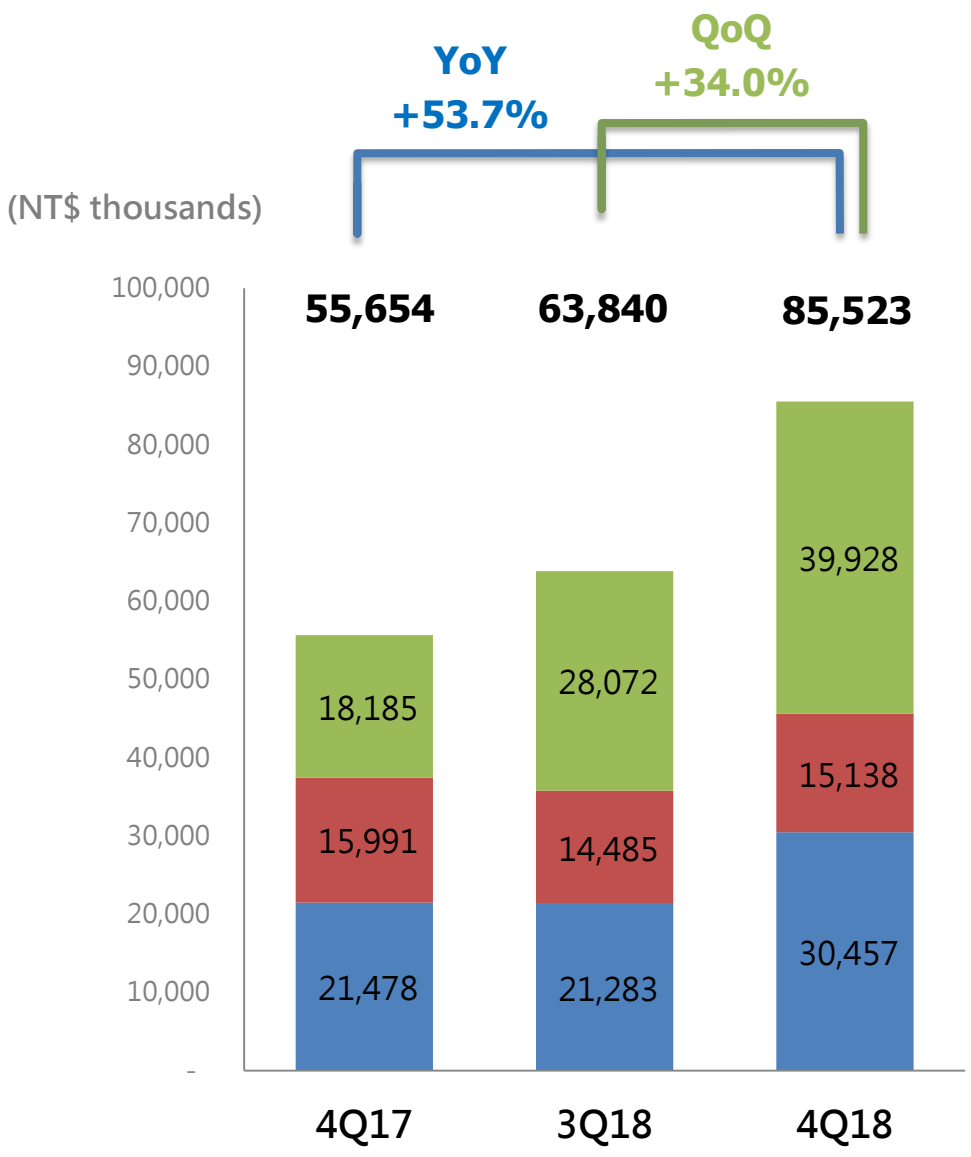


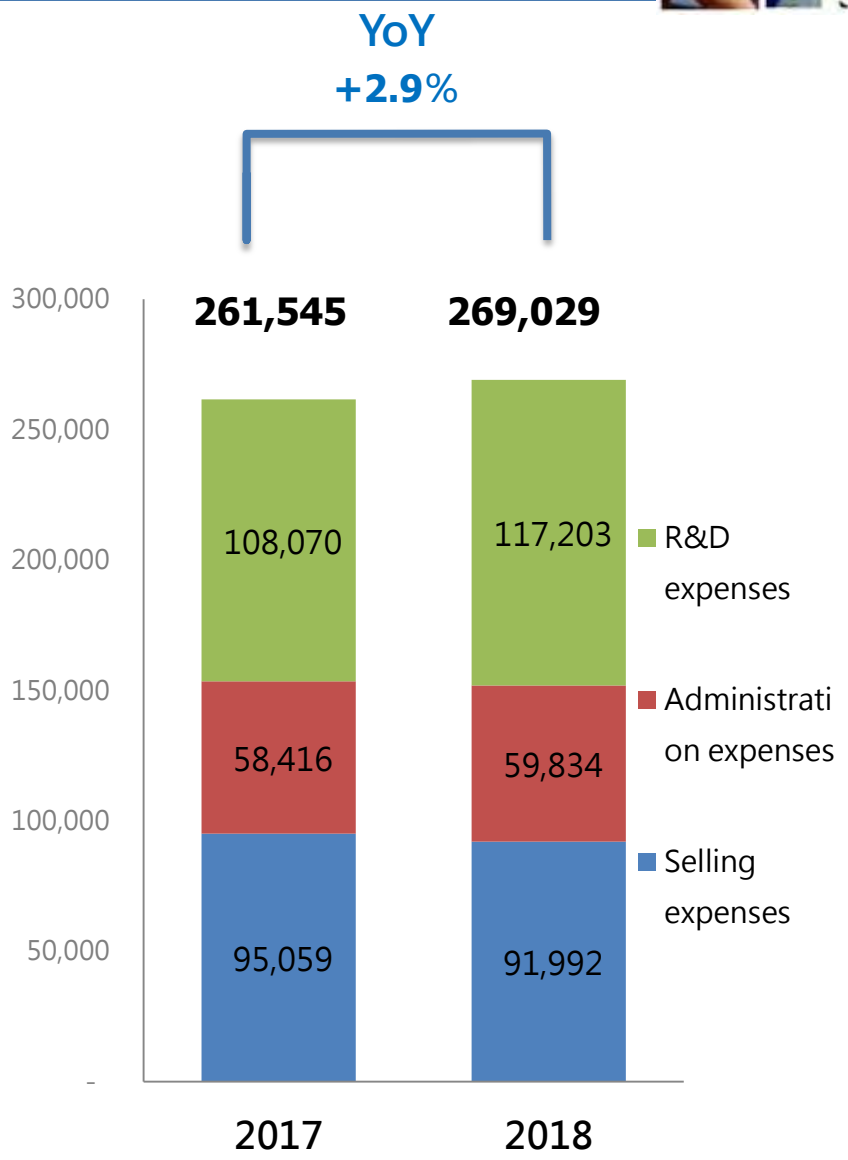
	4Q17	3Q18	4Q18
Gross Profit	56,798	56,217	125,574
Gross Margin	99.59%	99.74%	99.96%



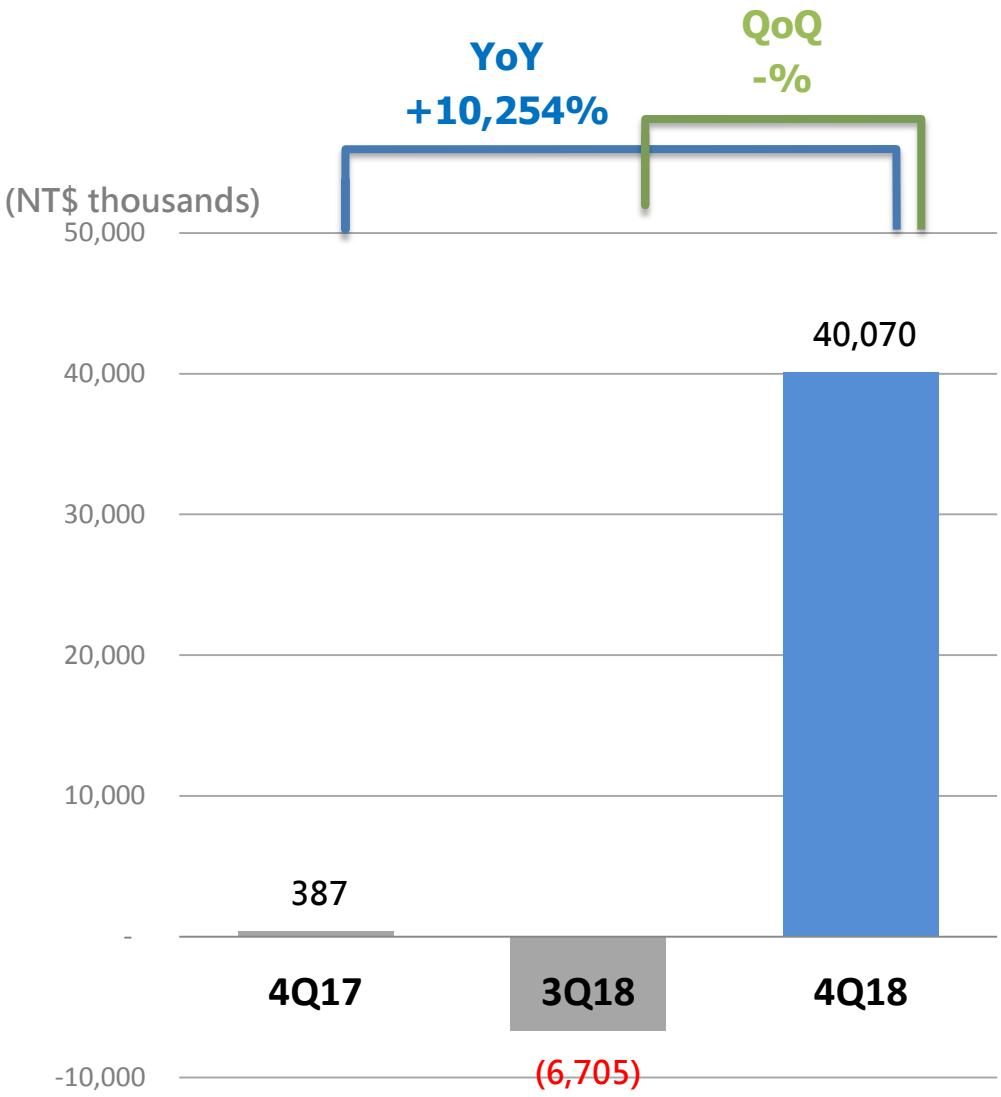
	2017	2018
Gross Profit	288,437	304,340
Gross Margin	99.68%	99.86%

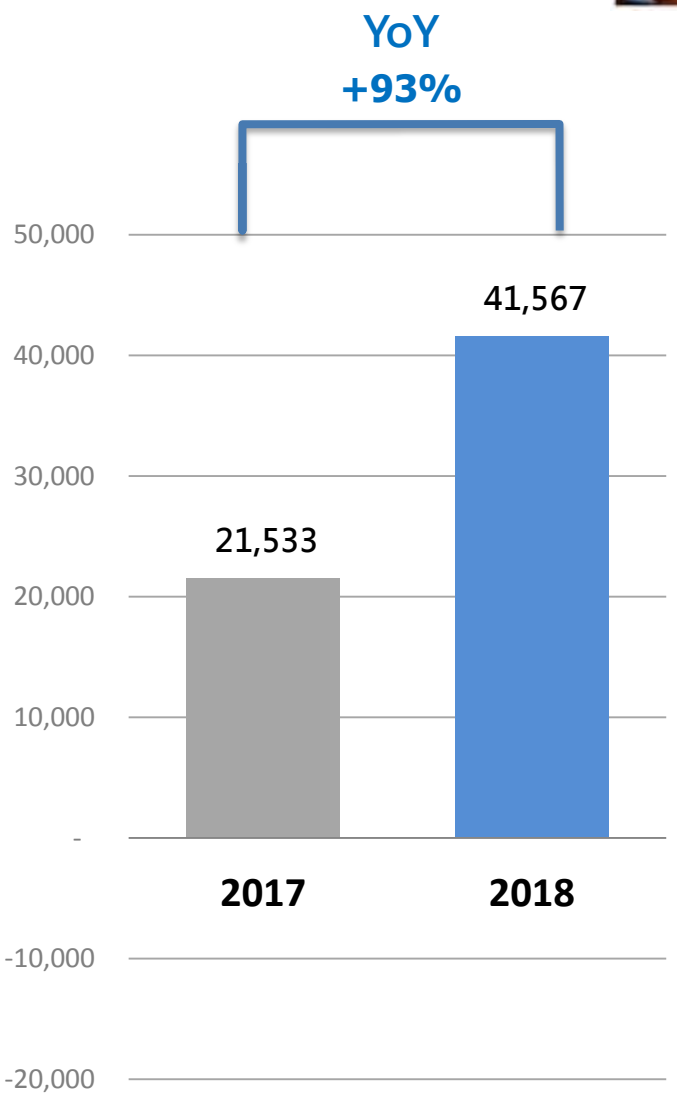
Consolidated Operating Expenses



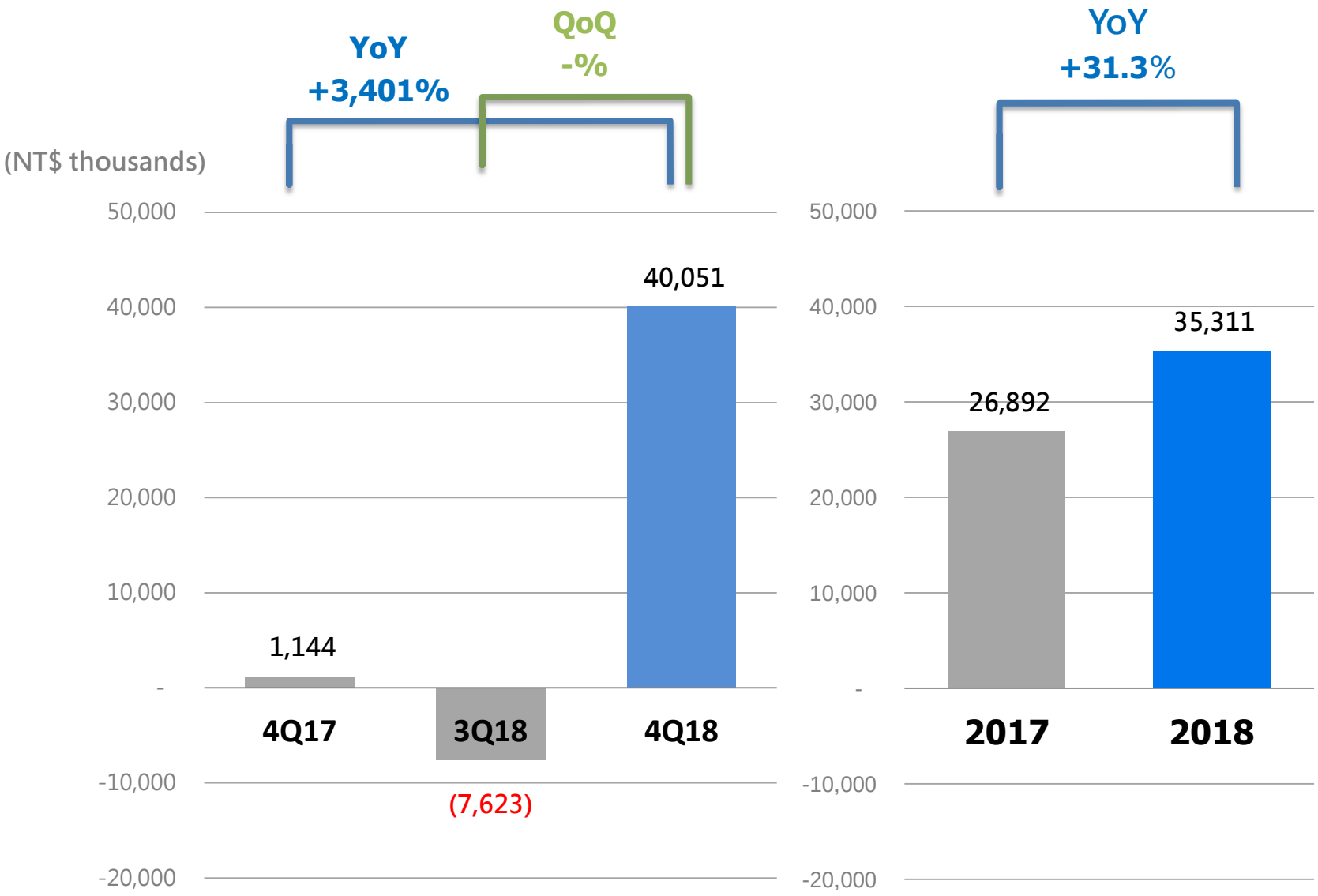


Consolidated Net Income

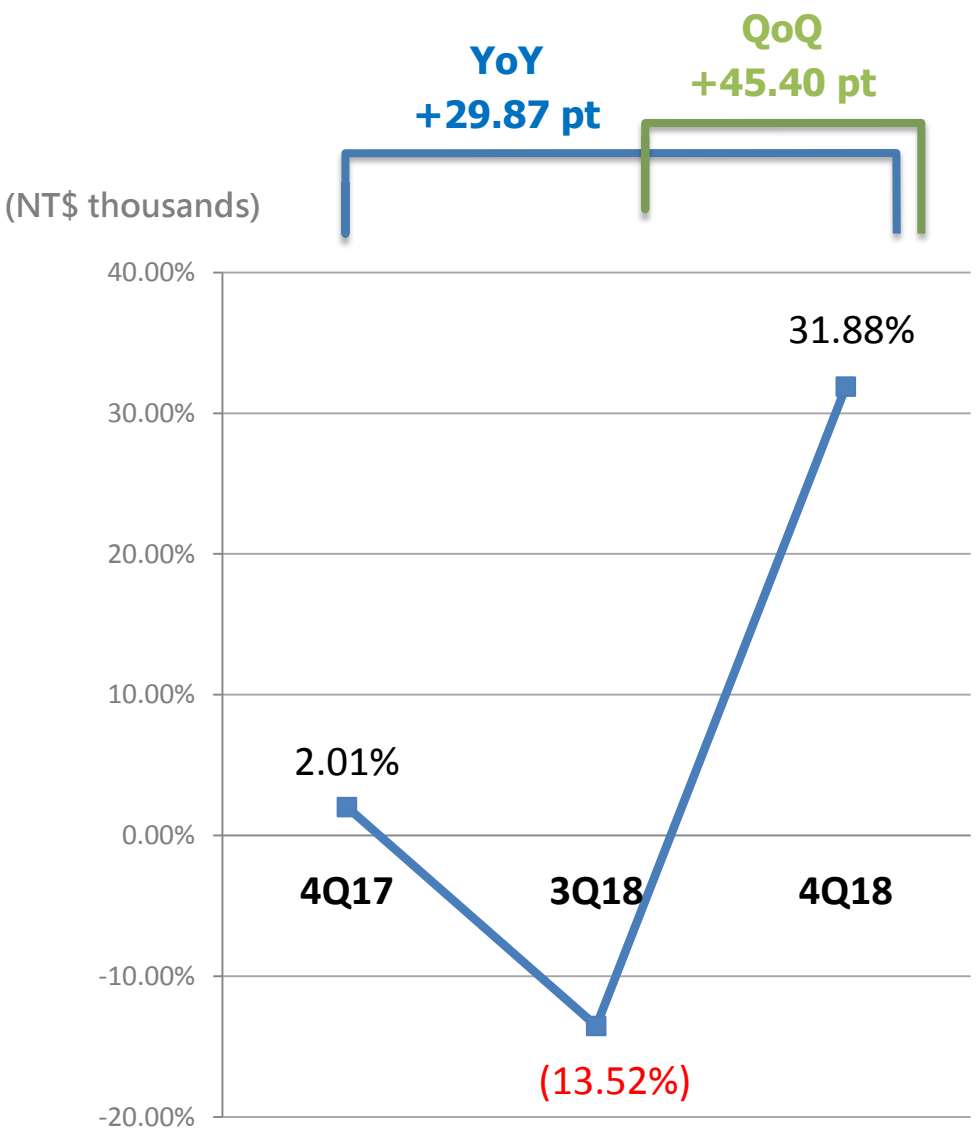


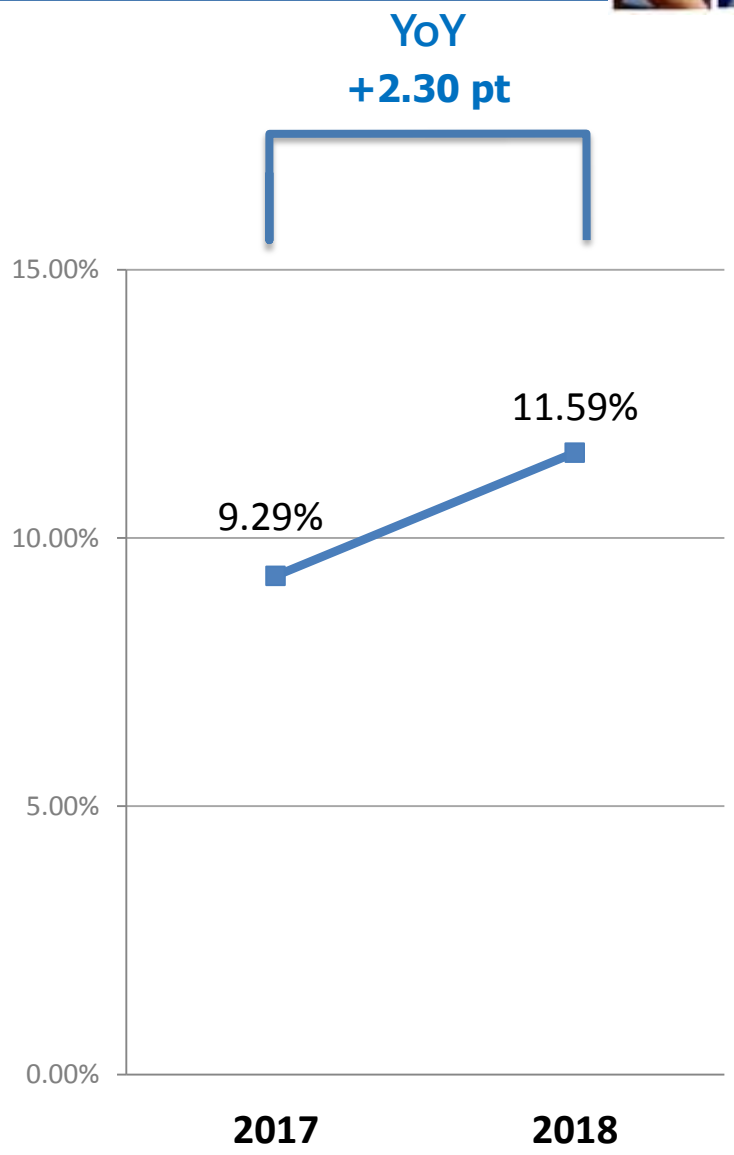


Consolidated Operating Income

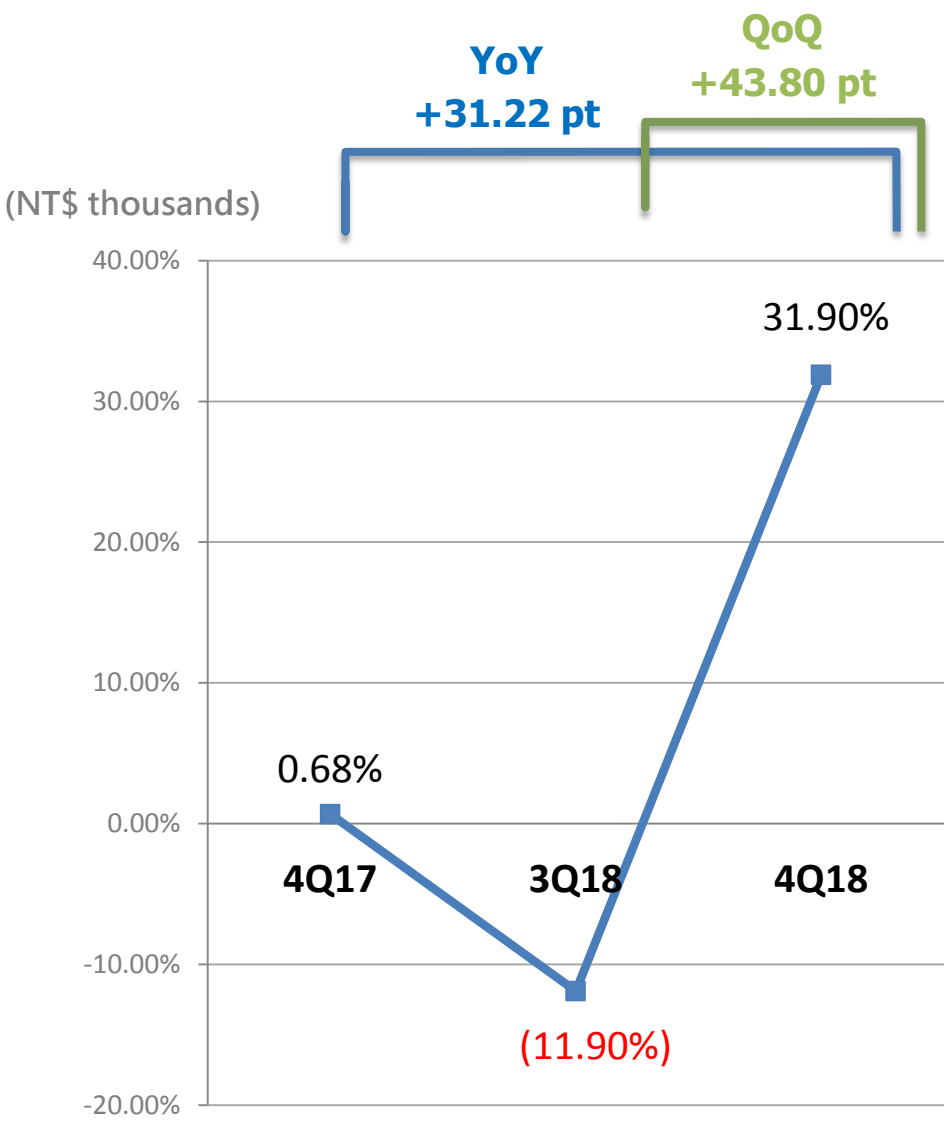


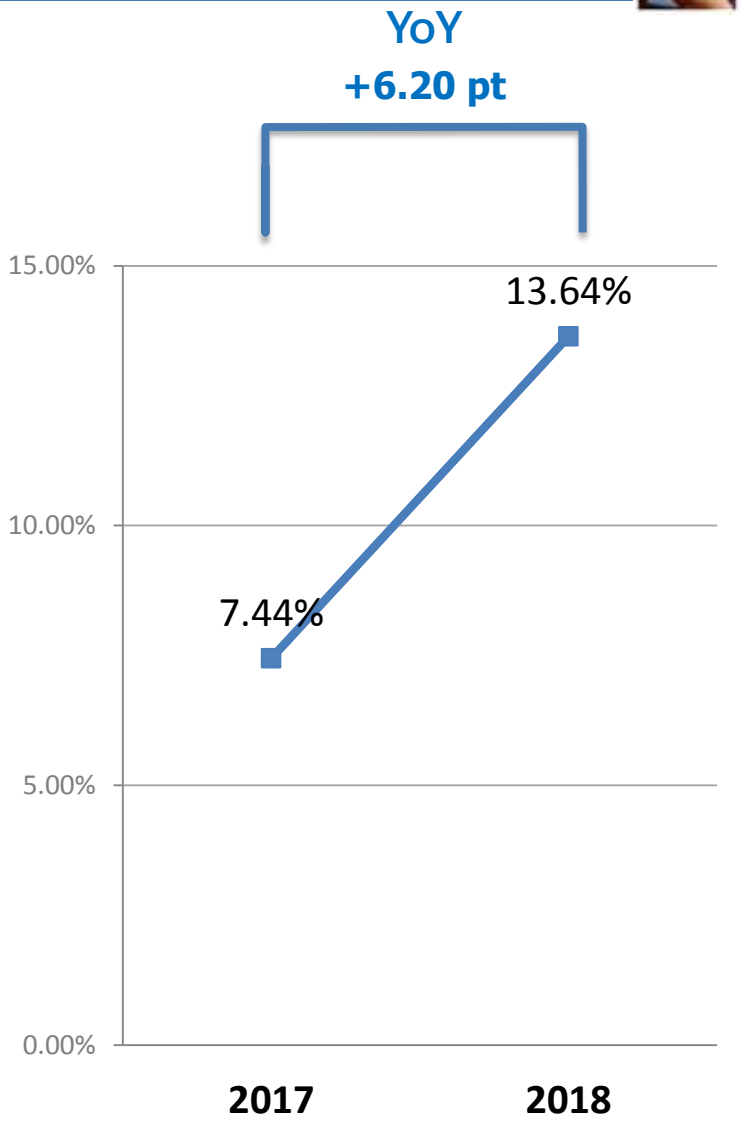
Consolidated Operating Margin



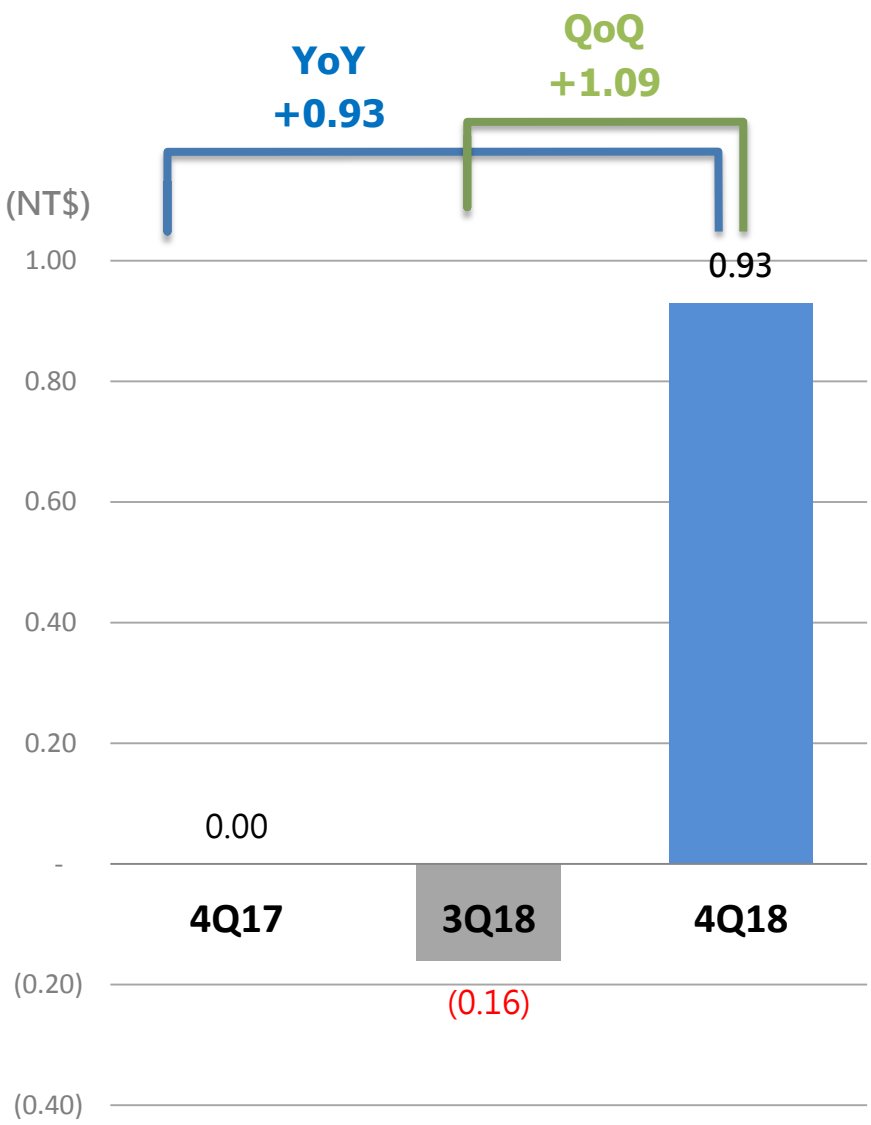


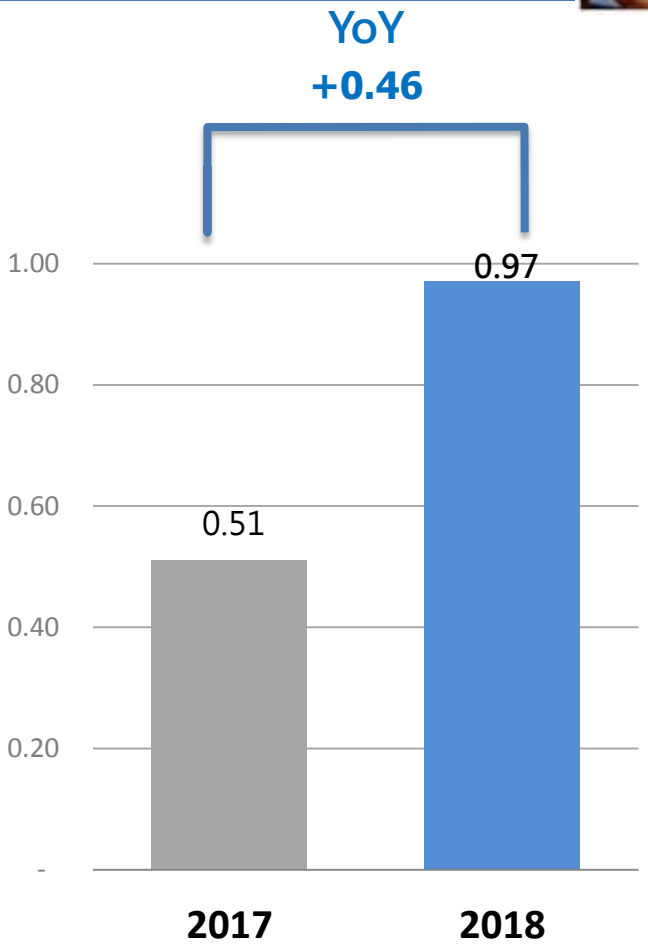
Consolidated Net Profit Margin





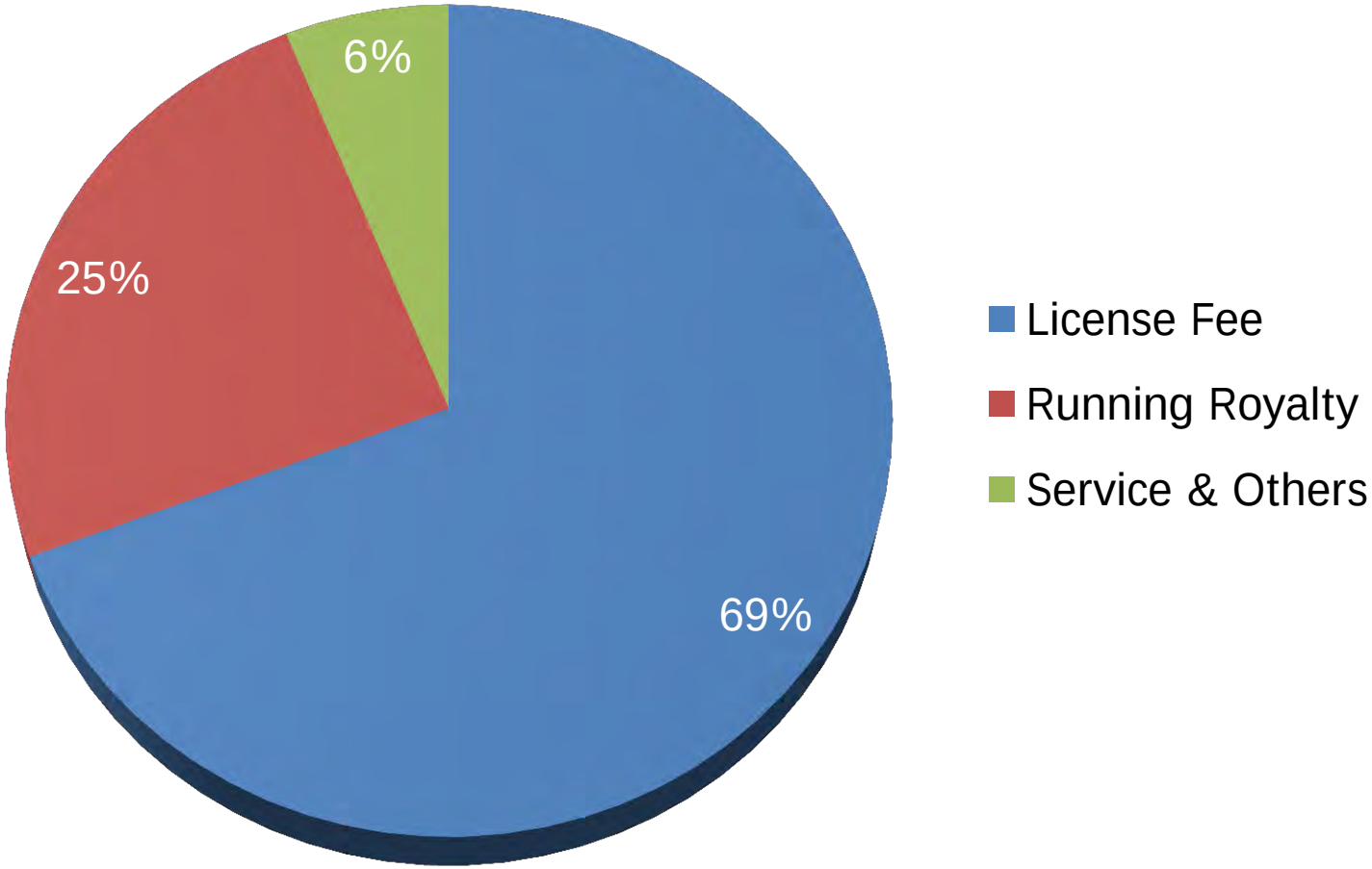
Consolidated Earnings Per Share



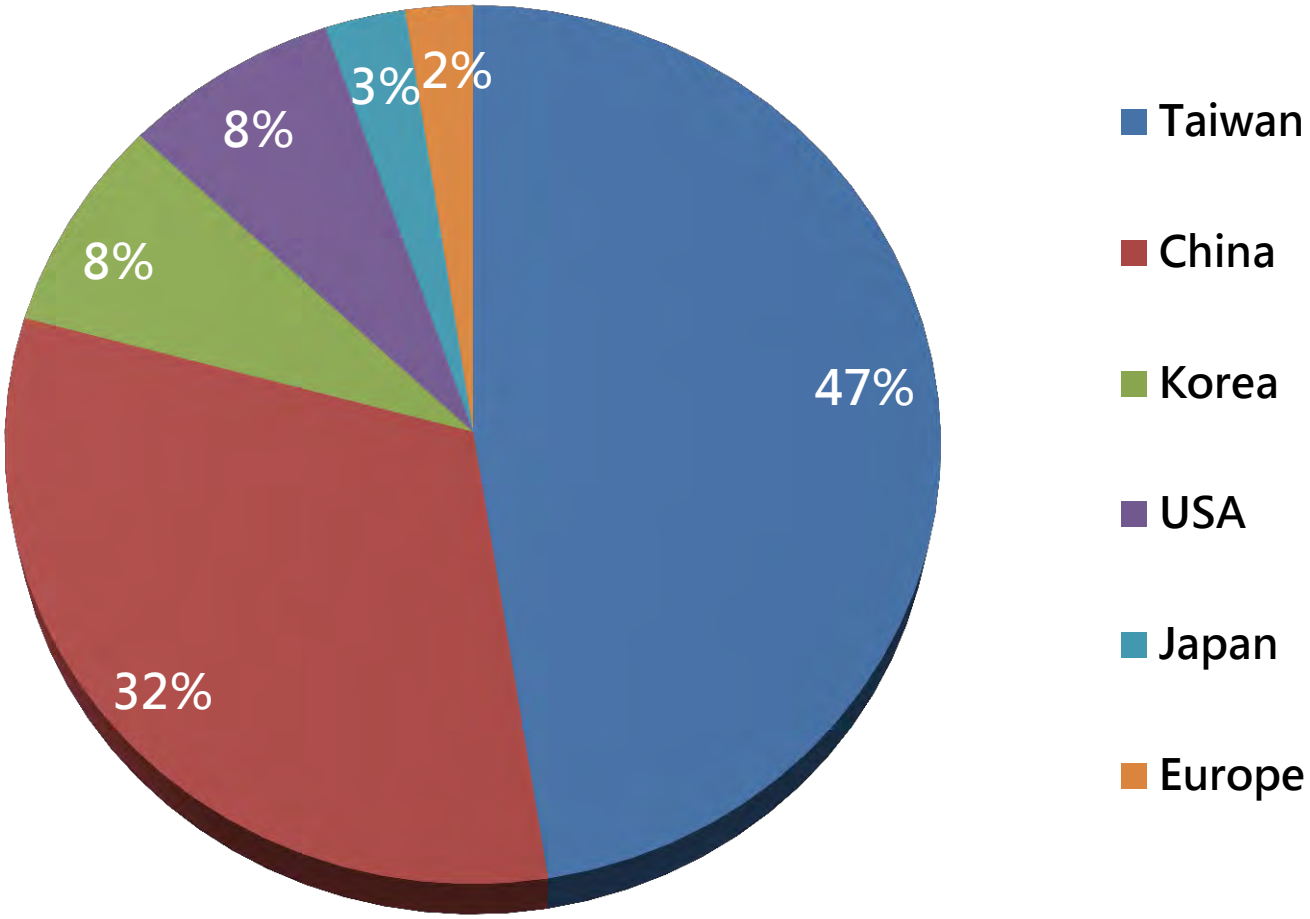


Revenue Analysis by Payment Model

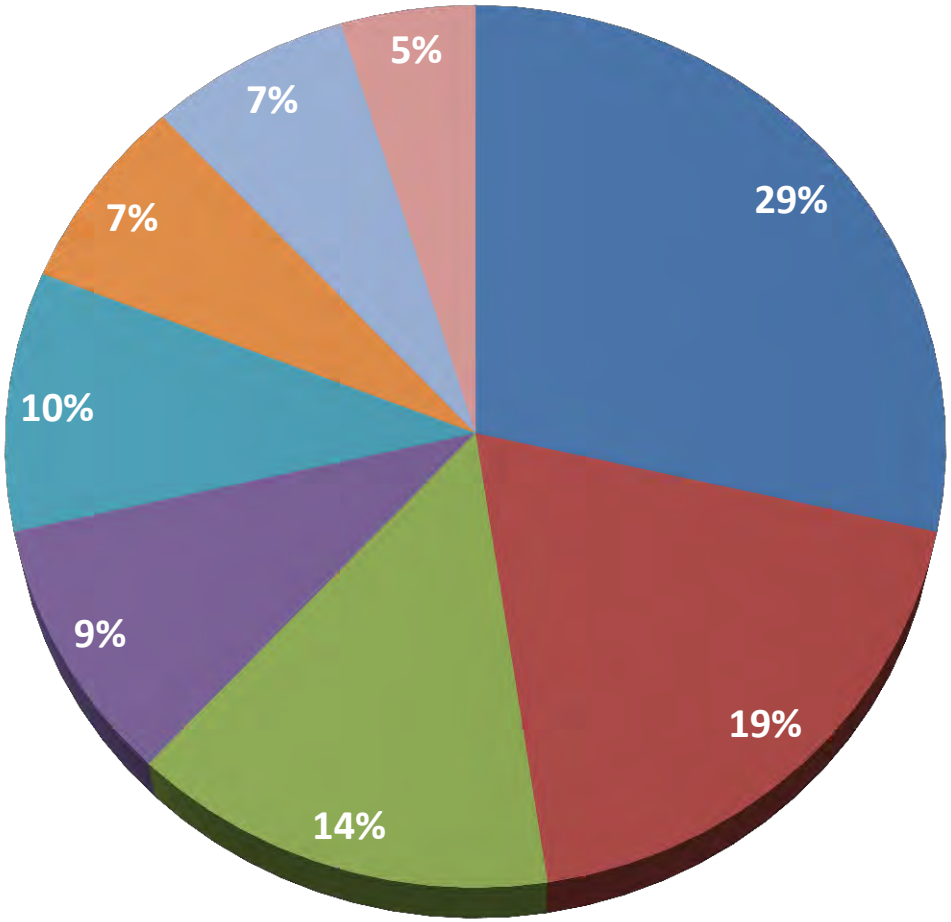
(2018/01-12 New Agreements: 42)



Revenue Analysis by Region

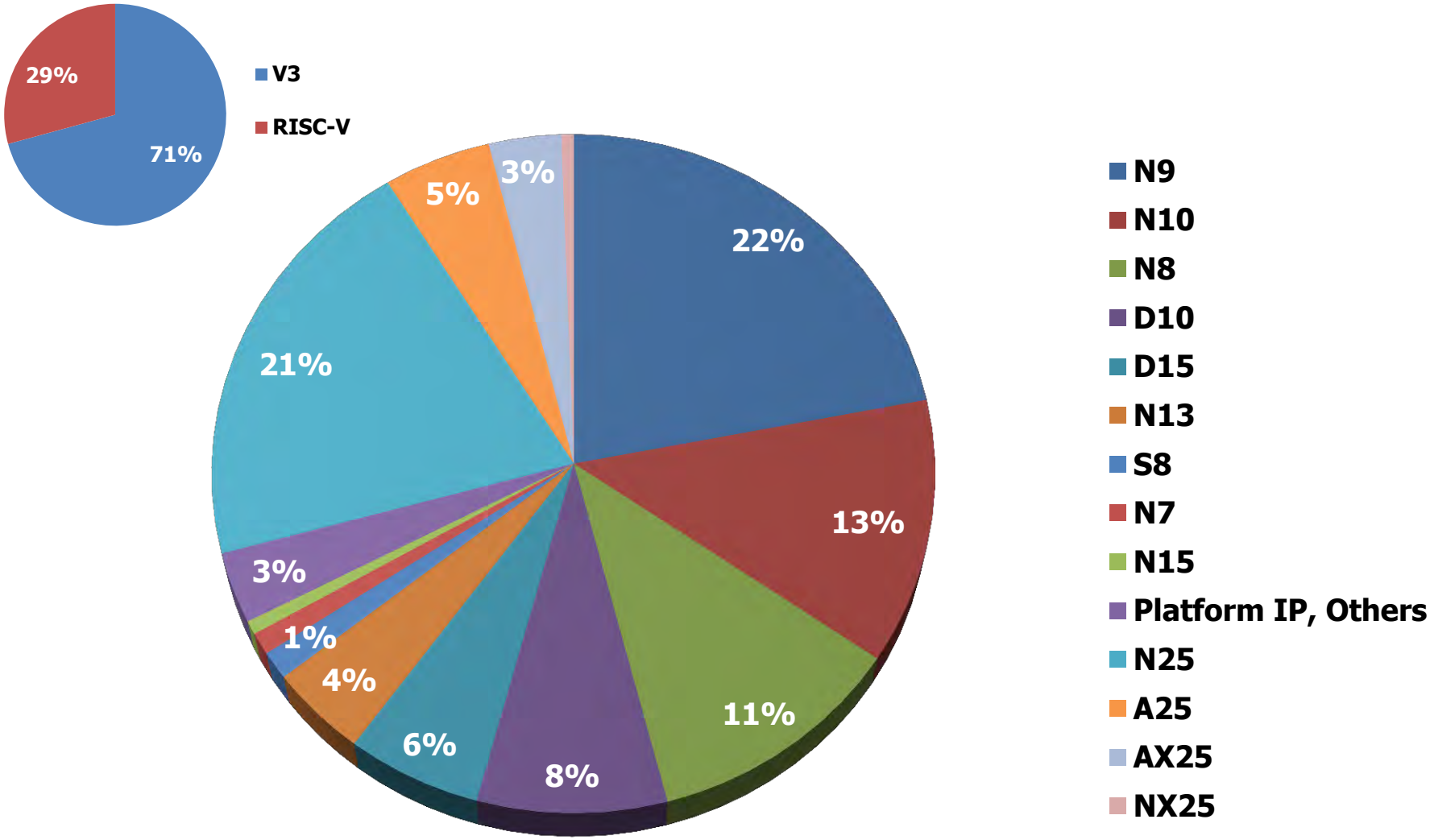


Customer Application Analysis

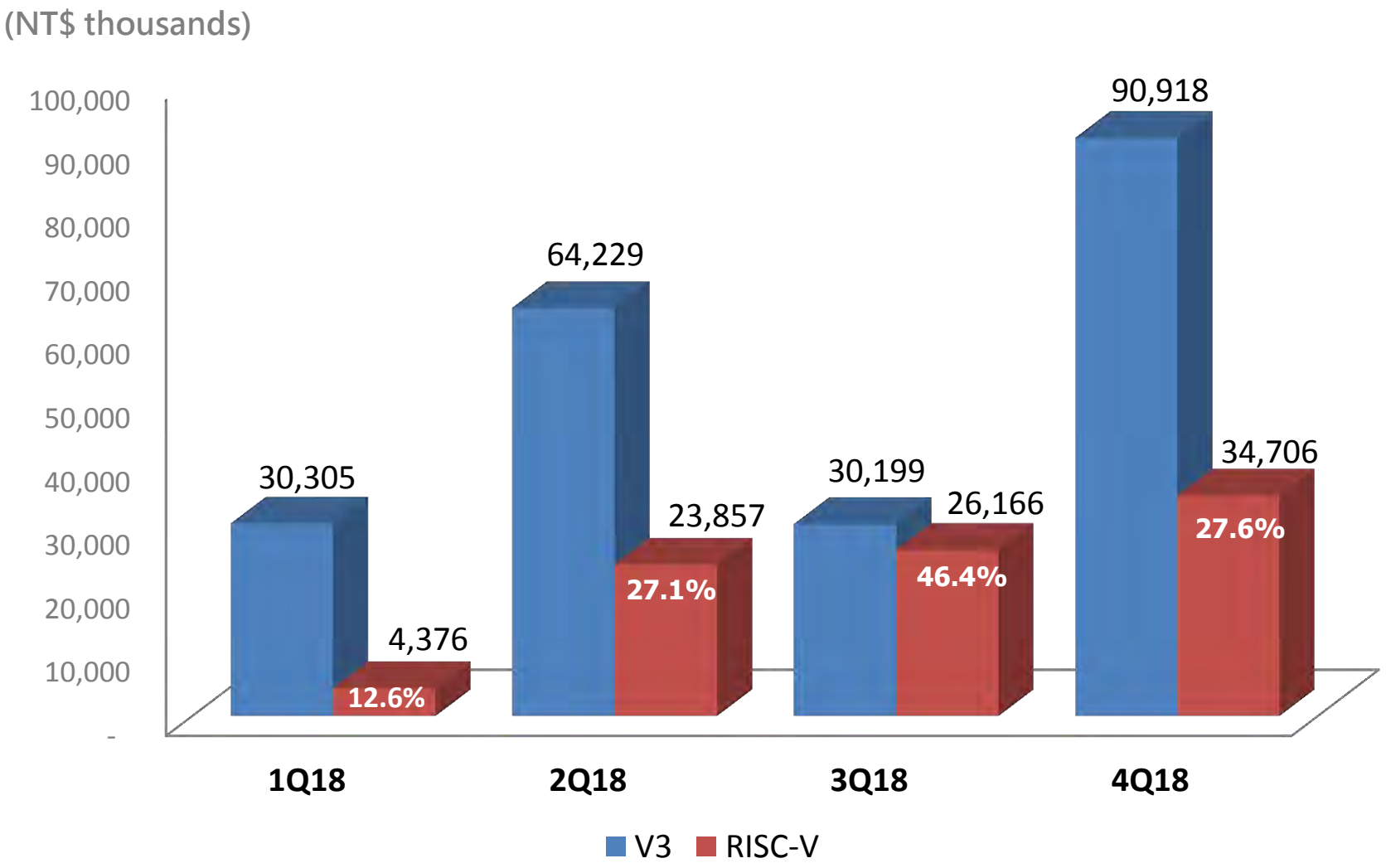


*Based on agreement number

Revenue Analysis by Product



2018 Revenue Analysis - RISC-V



Product Application

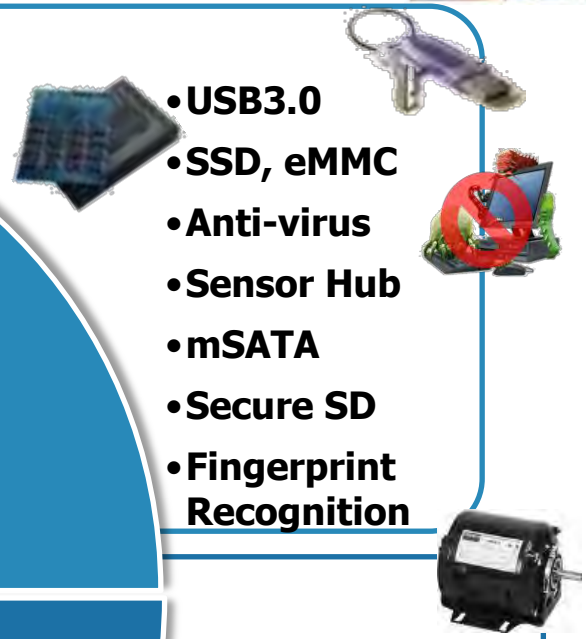
Andes Update

- A 14-year-old public CPU IP company
- >1B Andes-Embedded SoC shipped in 2018. >3.6B cumulatively.

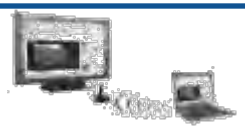
- A founding member of the RISC-V Foundation
- A major open source maintainer/contributor
- Active involvement in standard extensions
  - Chair of P-extension (Packed DSP/SIMD) Task Group
  - Co-chair of Fast Interrupt Task Group

Example Applications of Andes-Embedded™ SoC

- Touch Screen
- eBook/eDictionary
- Power management
- Bio-medical device
- CMMB
- MCU
- TCON



- USB3.0
- SSD, eMMC
- Anti-virus
- Sensor Hub
- mSATA
- Secure SD
- Fingerprint Recognition



- Wireless display
- WiFi, Bluetooth
- GPS, GPON, NFC
- Gateway/router
- Portable Karaoke
- Sigfox LPWAN
- IoT Cat0 base station
- IoT MCU • ESL
- Smart Meter • Smart Lighting

- Motor Control
- Wireless Charger
- Surveillance
- Barcode scanner
- ADAS
- VEDR
- 4K2K CODEC
- 8K4K CODEC

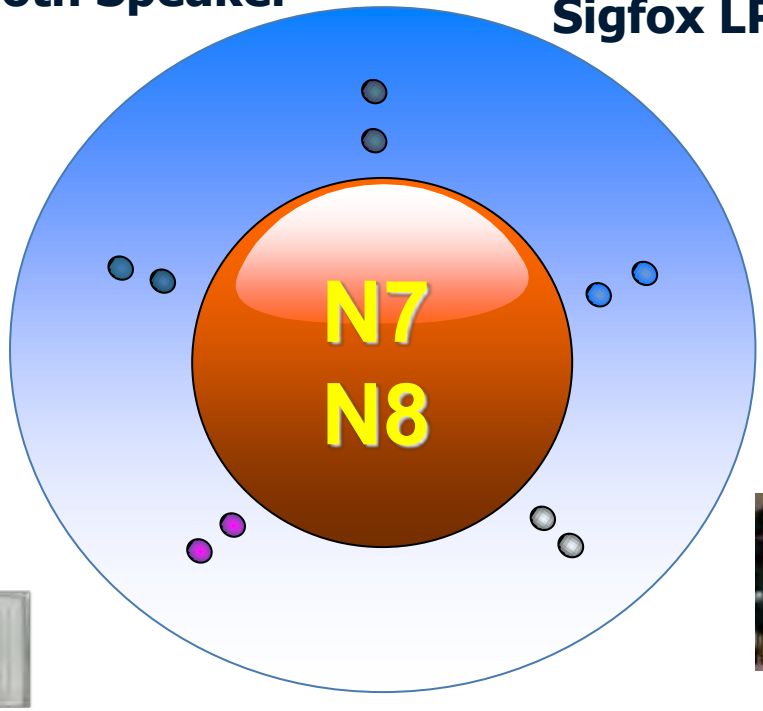
and more.....

IoT Application -1

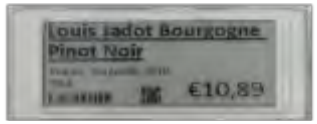
Bluetooth Speaker

Sigfox LPWAN

Healthcare device



Wearable device



Electronic price tags

Sensor Hub

IoT Application -2

Wearable devices

Drone

Portable Karaoke

N9
D10

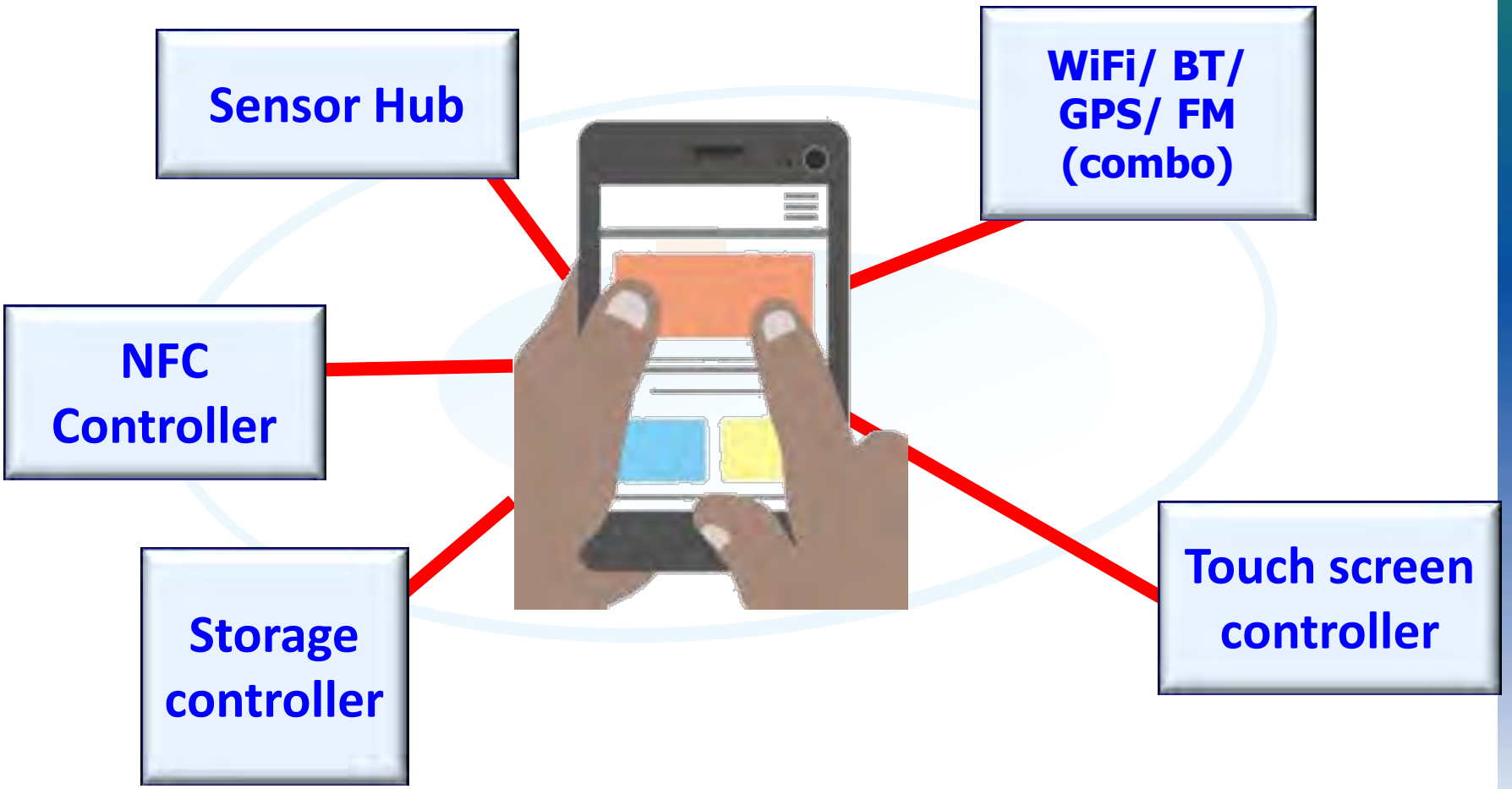
WiFi/GPS/FM/Bluetooth combo

GPS/Beido in shared bikes

Contactless payment (NFC)

Andes Embedded in Smart Phones

1 in 5 Smart Phones are with Andes Embedded worldwide



Andes Embedded
in Consumer Devices, Cars and Datacenters

Switch:
MXIC Flash Ctlr

Echo Dot2:
Mediatek WiFi IoT

Bike Sharing:
GPS Ctrl

X-Trail:
ADAS Ctlr

- In leading machine learning computers for datacenter
- In tier-one switch routers for datacenter

- Recent applications: 5G networking, 802.11ax, machine learning processors (using Andes Custom Extension, ACE)

New Products and Ecosystems

Product Lines

- New A-series Cores released in Andes Embedded Forum 2018

ANDES

RISC-V

Andes RISC-V Product Overview

Best extensions to RISC-V

AndeStar™ Architecture V5

RISC-V

Highly optimized design with leading PPA

AndesCore™ Processors

AndeSight™ Tools

Professional IDE with high code quality

Andes Embedded™

Handy peripheral IPs to speed up SoC construction

Extensive SW stacks from bare metal, RTOS to Linux

AndeShape™ Platforms

AndeSoft™ Stacks

V5 AndesCore™ Processors

N22

N25F/NX25F

A25/AX25

A25MP/AX25MP

Bring Andes Strength to RISC-V Core Family

- Architecture beyond the kernel for diversified requirements
- Efficient processor pipeline for leading PPA
- Platform IP support to help speed up SoC construction
- AndeSight IDE, and compiler/library optimizations
- RTOS and Linux support, and middleware (such as IoT stacks)
- Commercial-grade verification for all products
- Mass production experience with high quality deliverables
- Professional supporting infrastructure

The Latest Product Families

Launch of RISC-V Core IP Series

Cache-Coherent Multicores

A25MP[a]
V5, 32b, 1~4 Cores
L2 Cache Coherence
DSP, MMU, FPU, ACE ...

AX25MP[a]
V5, 64b, 1~4 Cores
L2 Cache Coherence
DSP, MMU, FPU, ACE ...

Linux and FPU/DSP

A25
V5, 32b, 5-stage, >1.2GHz,
MMU/PMP, DSP, FPU, ACE
...

AX25
V5, 64b, 5-stage, >1.2GHz,
MMU/PMP, DSP, FPU, ACE
...

Fast/Compact, FPU/DSP

D25F: +DSP

N25F
V5, 32b, 5-stage, >1.2GHz
PMP, FPU, ACE...

NX25F
V5, 64b, 5-stage, >1.2GHz
PMP, FPU, ACE...

Slim and Efficient

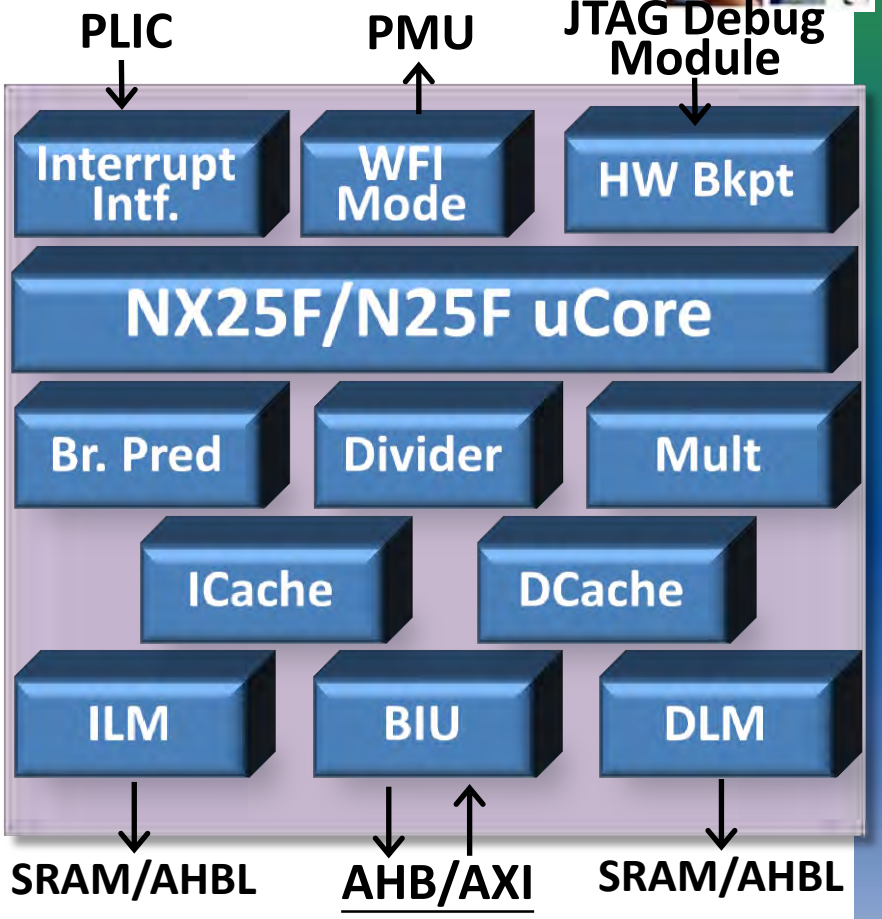
N22
V5/V5e, 32b, 2-stage
800MHz, 16/32 GPR

D22F
V5/V5e, 32b, 2-stage
800MHz, 16/32 GPR, DSP,
FPU

a. A25*MP: available Q1/2019
b. 28HPC+ RVT, SS, 0.81V, 0C, with I/O constraints.

V5 AndesCores: 25-series

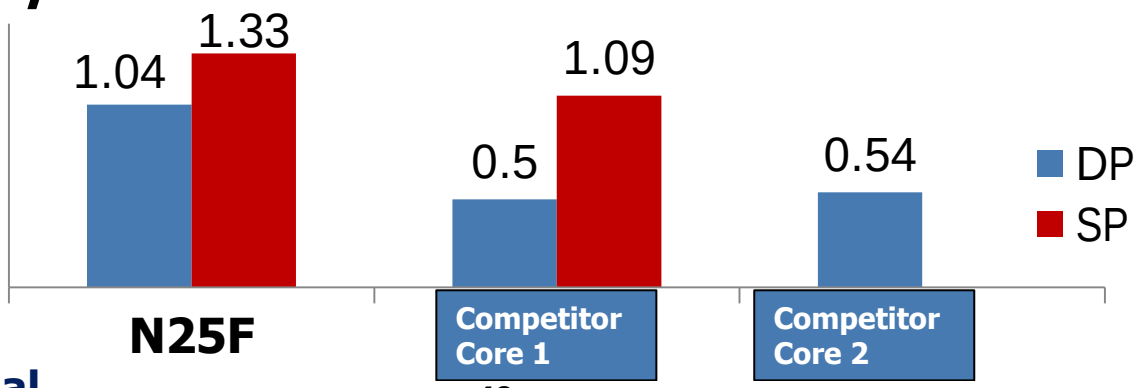
- **N25F: 32-bit, NX25F: 64-bit**
  - From scratch for the best PPA
  - Very configurable
- **AndeStar V5 ISA**
- **5-stage pipeline**
- **Configurable multiplier**
- **Optional branch prediction**
- **Flexible memory subsystem**
  - I/D Local Memory (LM): to 16MB
  - I/D caches: up to 64KB, 4-way
  - Optional parity or ECC
  - Hit-under-miss caches
  - load/store: unaligned accesses



- **N25F sample configurations @TSMC 28HPC+ RVT:**
  - Small config: 37K gates, 1.0 GHz (worst case)
  - Large config: 130K gates, 1.2GHz (worst case)
  - **Best-in-class Coremark: 3.58/MHz**

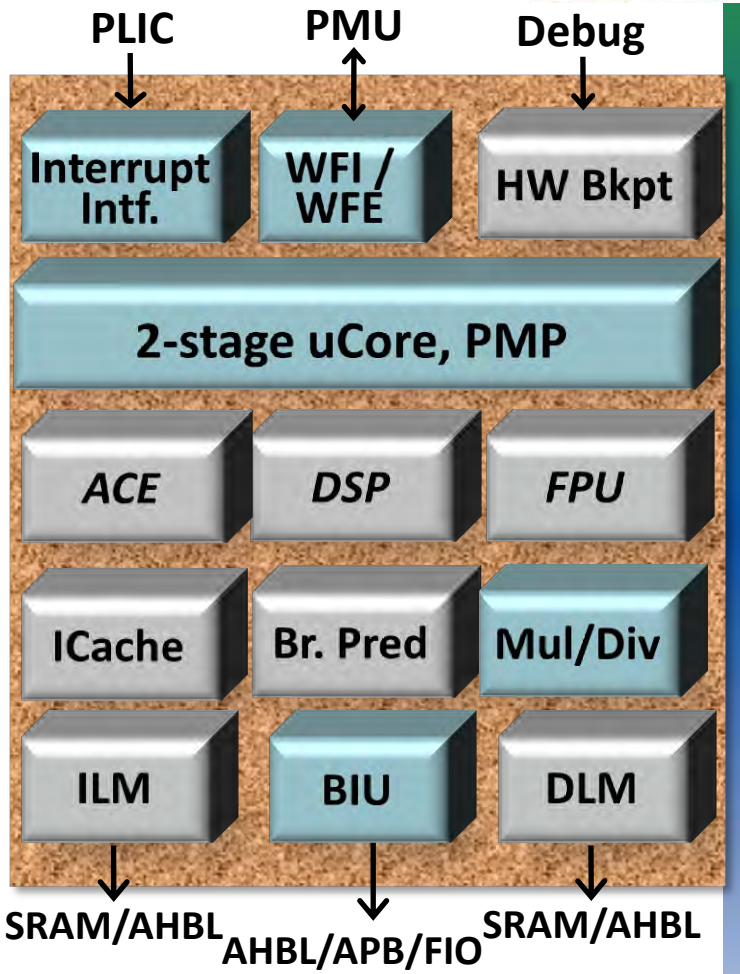
V5 AndesCores: 25-series

- **Fast-n-small for control tasks in AR/VR, networking, storage, AI**
- **N25F/NX25F: +FPU**
  - +, −, x, x+, x−: pipelined 4 cycles
  - ÷, √ : run in the background
    - ◆15 for SP, 29 for DP
  - FP load/store: support HP
- **A25/AX25: +FP +Linux**
  - Support RISC-V MMU and S-mode
  - 4 or 8-entry ITLB and DTLB
  - 4-way 32~128-entry Shared-TLB
- **Whetstone/MHz**:



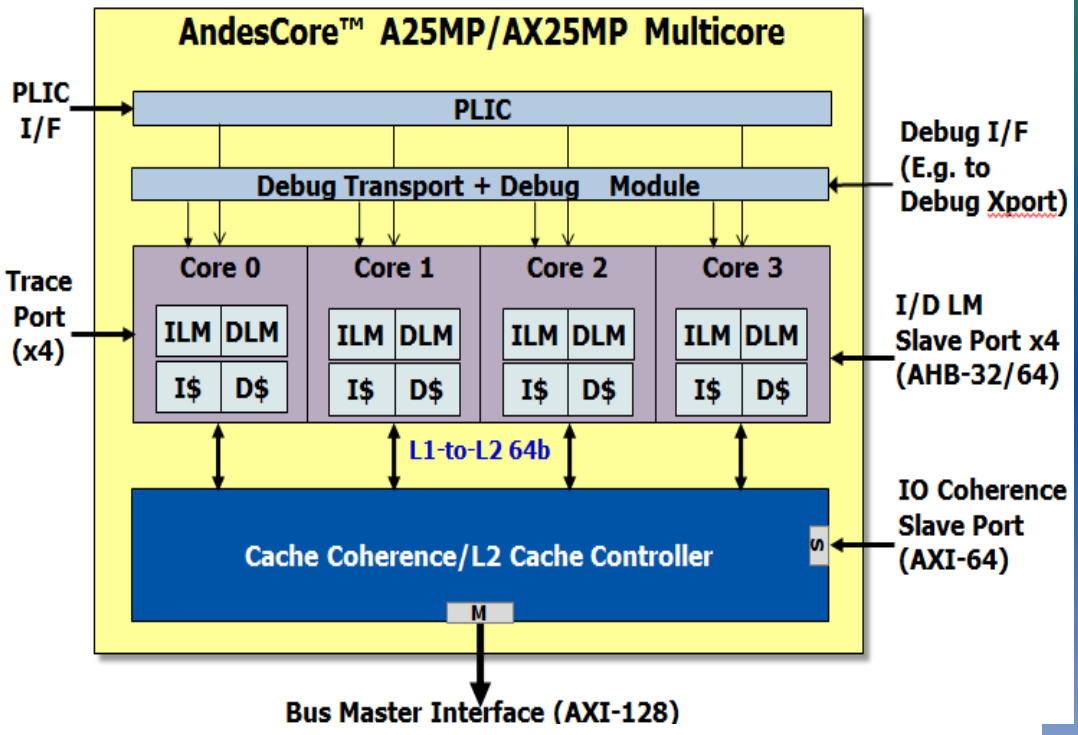
V5 AndesCores: 22-series

- **AndeStar V5 or V5e ISA**
  - RV32-IMC or RV32-EMC
  - Plus Andes extension
- **2-stage pipeline with AHB-lite main bus**
- **Rich baseline options:**
  - I/D Local Memory (1KB~512MB), I cache
  - Fast or small multiplier, branch predictions
  - Up to 16-entry PMP, StackSafe
  - M-mode, or M+U-mode
  - APB private peripheral port, fast IO port
  - WFI, WFE, and PowerBrake
  - Vectored and preemptive interrupt controller
- **Advanced options: *ACE, DSP, FPU***
- **28nm PPA:**
  - **>750 MHz** (worst case)
  - **<15K gates** (minimal)
- **Best per-MHz performance:**
  - **1.8 DMIPS** (no inline)
  - **3.97 Coremark**



A(X)25MP Cache-Coherent Multicore

- **1/2/4 A25 (32-bit)/AX25 (64-bit) CPUs**
  - RV-IMACFD ISA, supporting SMP Linux
  - With the latest P-extension (DSP/SIMD ISA), Andes' contribution to RISC-V
- **Hardware Multicore Cache Coherence**
  - Support MESI cache coherence protocol by ACU (Andes Coherence Unit)
  - Support I/O coherence without data caches
- **Level-2 Cache Controller**
  - 0/128/256K...2MB, 32-byte line, 16-way
  - ECC, SECDED support
- **Bus Interfaces**
  - AXI bus master interface
  - Local memory slave port, for each A25/AX25 CPU
  - I/O coherence slave port
  - MP subsystem vs. bus interface synchronous N:1 clock ratio
- **Platform Level Interrupt, Debug and Trace Support**



ACE: Andes Custom Extension

Verilog user.v

concise RTL

semantics, operands, test-case spec

script user.ace

COPILOT

Custom-OPtimized Instruction deveLOpment Tools

Extended Tools + Compiler Asm/Disasm Debugger IDE

Extended ISS + CPU ISS (near-cycle accurate)

Extended RTL + CPU RTL

Extensible Baseline Components

Automated Env. For Cross Checking

Test Case Generator

Extended RTL

Extended ISS

Executable or library

Source file

Aggressive in RISC-V Community

Foundation Task Groups (partial list)

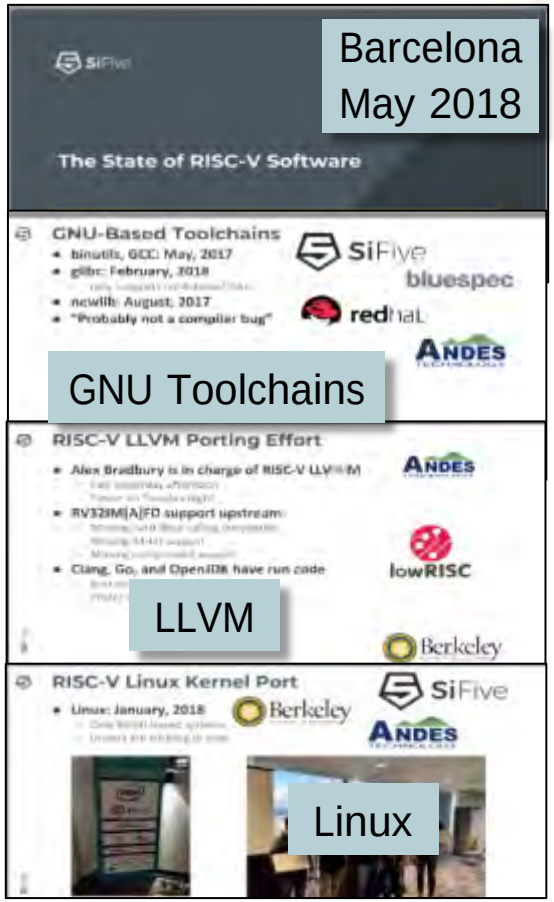
- **Contributing hardware architecture extensions**
  - **Chair of the P-extension (Packed SIMD/DSP) Task Group**
  - **Co-chair of Fast Interrupts Task Group**
  - **Closely reviewing activities of other Task Groups**

Andes Helps Strengthen RISC-V Ecosystem

- More choices for customers are good
- Andes works closely with partners to grow RISC-V ecosystem

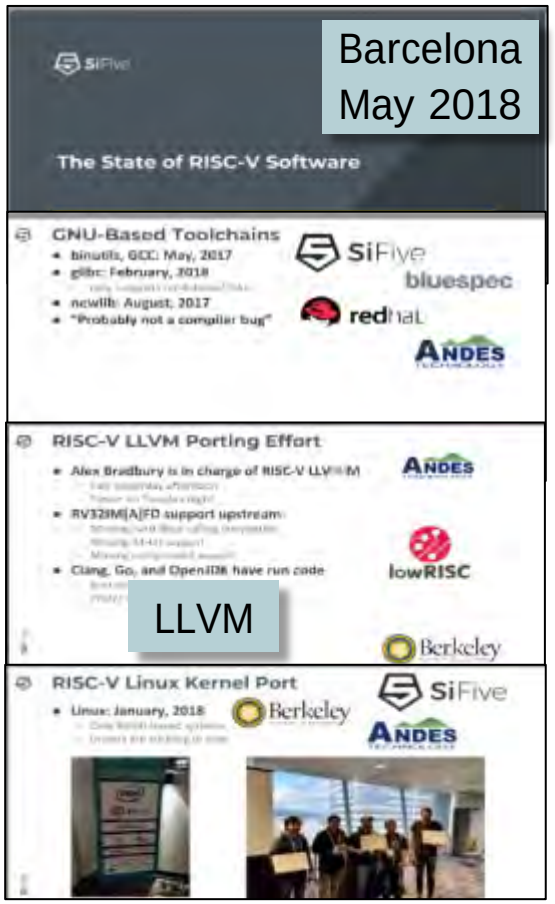
RISC-V Software Ecosystem: GNU Toolchain

- **GCC, binutils**: May, 2017
- **Newlib**: Aug, 2017
- **Glibc (rv64i)**: Feb, 2018
- **GDB**: Mar, 2018
- **OpenOCD**: July, 2018
- **Glibc (rv32i)**:
  - Submitted in July 2018 (by Andes)
  - Review in progress



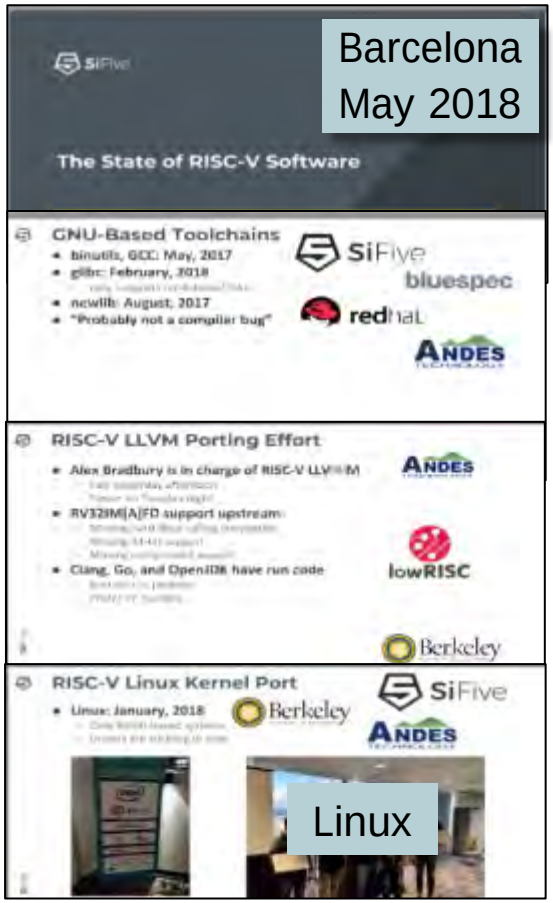
RISC-V Software Ecosystem: LLVM Compilation

- **LLVM**:
  - RV32IMAFDC: June, 2018
  - Relaxation: May, 2018 (by Andes)
  - 64b support: Nov, 2018
  - Missing hard-float calling convention
- **compiler-rt**: Mar, 2018
- **LLD**: Aug, 2018 (by Andes)
  - Initial port (relocation and TLS) in Oct. 2017
  - Dynamic linking review in progress since Oct, 2017
  - Missing link-time relaxation



RISC-V System Software Ecosystem: Linux

- **U-boot**: Jan, 2018 (by Andes)
- **Kernel (rv64i)**: Jan, 2018
- **Key utilities**: (by Andes)
  - Perf: Feb, 2018
  - Kernel Module: May, 2018
  - Ftrace: May, 2018
- **Kernel (rv32i)**: Jun, 2018 (by Andes)
- **Kernel with CONFIG_FPU**: Oct, 2018 (by Andes)



Andes Position in RISC-V

- Complete product portfolio
- Reliable RISC-V core IP provider
- RISC-V cores that run Linux
- Extreme low power consumption, high computing efficiency
- World's leading Customer-Extension Capable RISC-V Core

2018 RISC-V Design Win

- **Sixteen design wins for Andes RISC-V Core IPS:**
  - **NX25: Enterprise SSD (Taiwan)**
  - **N25: AI (China w/ ACE), Blockchain (China), HD-PLC (Japan), SSD (China), Fingerprint (Taiwan), AI (China x2), TDDI (Taiwan), SD/eMMC (Taiwan), Research/Academic (Taiwan x2)**
  - **N25/AX25: FPGA for AI (US)**
  - **AX25: FPGA for AI (China)**
  - **A25: 5G (US), Automotive (Korea)**
- **Thirteen design service providers joined Andes RISC-V Easy Start Program:**
  - **US x 3, Europe x1, Korea x 1, China x 3, Taiwan x 5**

Summary of AndesCores vs. Competitors

AndesCore™	AndesCore/ Competitor Power Efficiency[1] (DMIPS/mW)	Competitors
N7	+42%	Cortex-M0+
N8	+43%	Cortex-M3
N9	+43%	Cortex-M3
D10	+48%	Cortex-M4
N13	+185%	Cortex-A5
N13	+45%	Cortex-R4
D15F	+121%	Cortex-M7

1. Power Efficiency is DMIPS/MHz divided by power consumption (mW/MHz) when running Dhrystone.

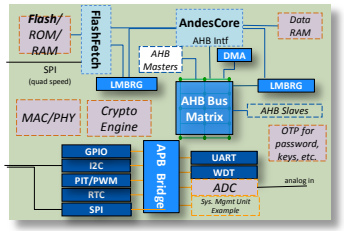
Two Ecosystems: Andes and Knect.me

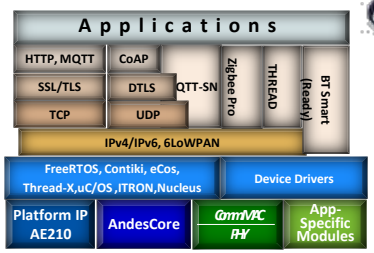
ANDES TECHNOLOGY

knectme™

Knect.me Ecosystem

- **Built up Ecosystem *knect.me* to help IoT Developing**
  - to **knect** solutions - Silicon IP's, SW stacks, tools, applications, systems and products
- **Includes:**
  - SoC IP Platforms
  - Software Stack
  - Development Boards
  - Development Tools
- **To Form a IoT League**
  - to **knect** chip vendors, partners, application developers, system vendors





Andes Awarded

ANDES TECHNOLOGY

Leader of the Emerging Technology

- "2018 Top25 emerging tech solutions provider"

— CIO Advisor Magazine

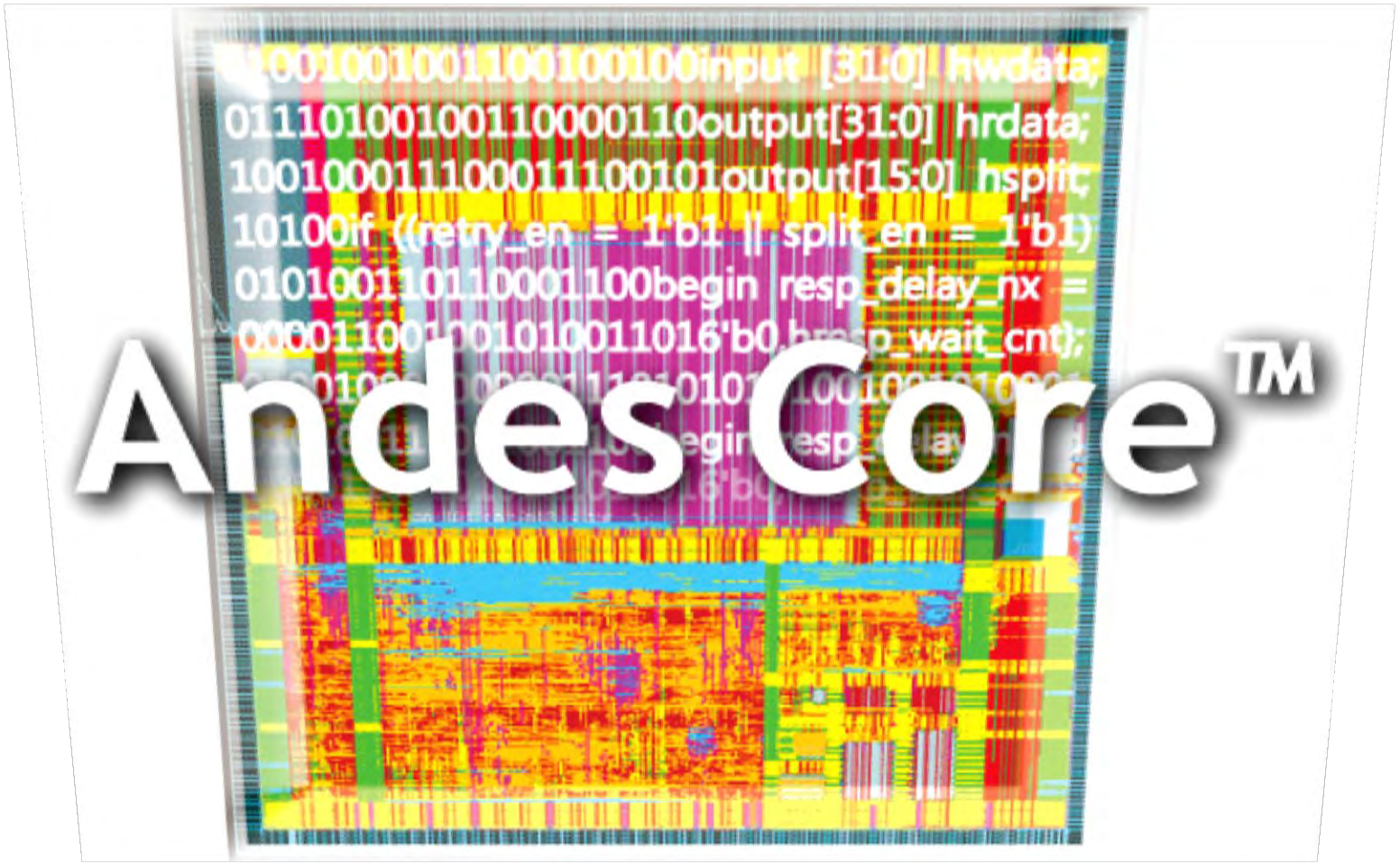
Concluding Remarks

ANDES TECHNOLOGY

Andes: Even Better Value in Future

- Andes revealed new RISC-V processor cores (N22, A(X)25MP, D25F) to fit in more applications from customers.
- Andes aggressively involved in RISC-V Foundation new technology development, contributing and leveraging RISC-V eco-system.
- Andes has successively signed thirteen contracts with design service houses in 2018 to authorize ASIC design to embed RISC-V core (Andes RISC-V Easy Start Program). Andes aim to sign up 20 design service houses worldwide in a few months. These contracts will create a win-win situation for Andes, design service houses and customers.

Thank You!



www.andestech.com

Q&A

AndeStar™ V5: New Generation of ISA Kernel