晶心科技股份有限公司
2018年法人說明會

Driving Innovations™

股票代號: 6533
2019/03/26

投資安全聲明

除簡報內所提供之歷史信息外，簡報事項係屬預測性陳述，受到風險及不確定性因素影響，可能造成實際結果與陳述內容發生不符，這些不確定性因素包括但不限於：天氣、競爭性產品及其定價的影響、產業及市場對半導體產品之供給及需求移轉、新產品大量量產之能力、技術急遽演進、半導體產業景氣以及整體經濟環境之變化。

簡報大綱

- 公司簡介
- 營運成果
- 產品應用
- 新產品及生態系統
- 近期獲獎
- 總結

公司簡介

晶心亮點

- 2005年3月設立於台灣新竹科學園區。
- 核心研發團隊來自於**AMD**, **DEC**, **Intel**, **MIPS**, **nVidia**, and **Sun**。
- 員工人數達160人；80%為工程師。
- **EETimes**評為全球60家最具潛力半導體新創公司。**(2012)**
- 獲得**TSMC 2015**年新的 **IP OIP Award** 。
- **RISC-V**基金會創始成員。 **(2016)**
- 股票於台灣交易所掛牌上市。**(2017**年 **3**月**)**

晶心任務

- 創新架構高效能/低功耗嵌入式處理器。

晶心利基

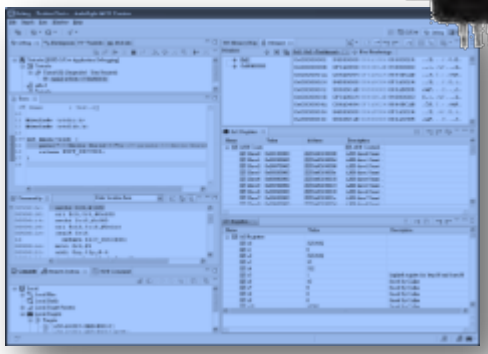
- **智能及環保之電子設備**
- **雲端應用,人工智慧及物聯網**

營運成果

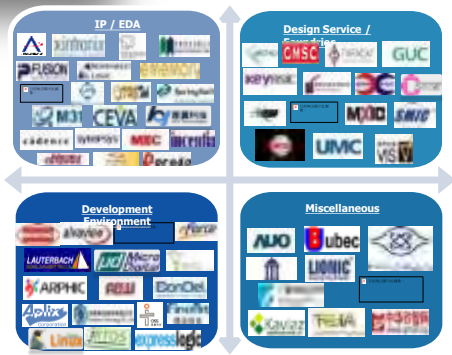
重要里程碑

- 全球授權客戶超過 160家
  - 台灣, 大陸, 韓國, 日本, 歐洲, 及美國
  - 授權合約超過246份

- AndeSight™ IDE:
  - 安裝次數超過 14,000 次

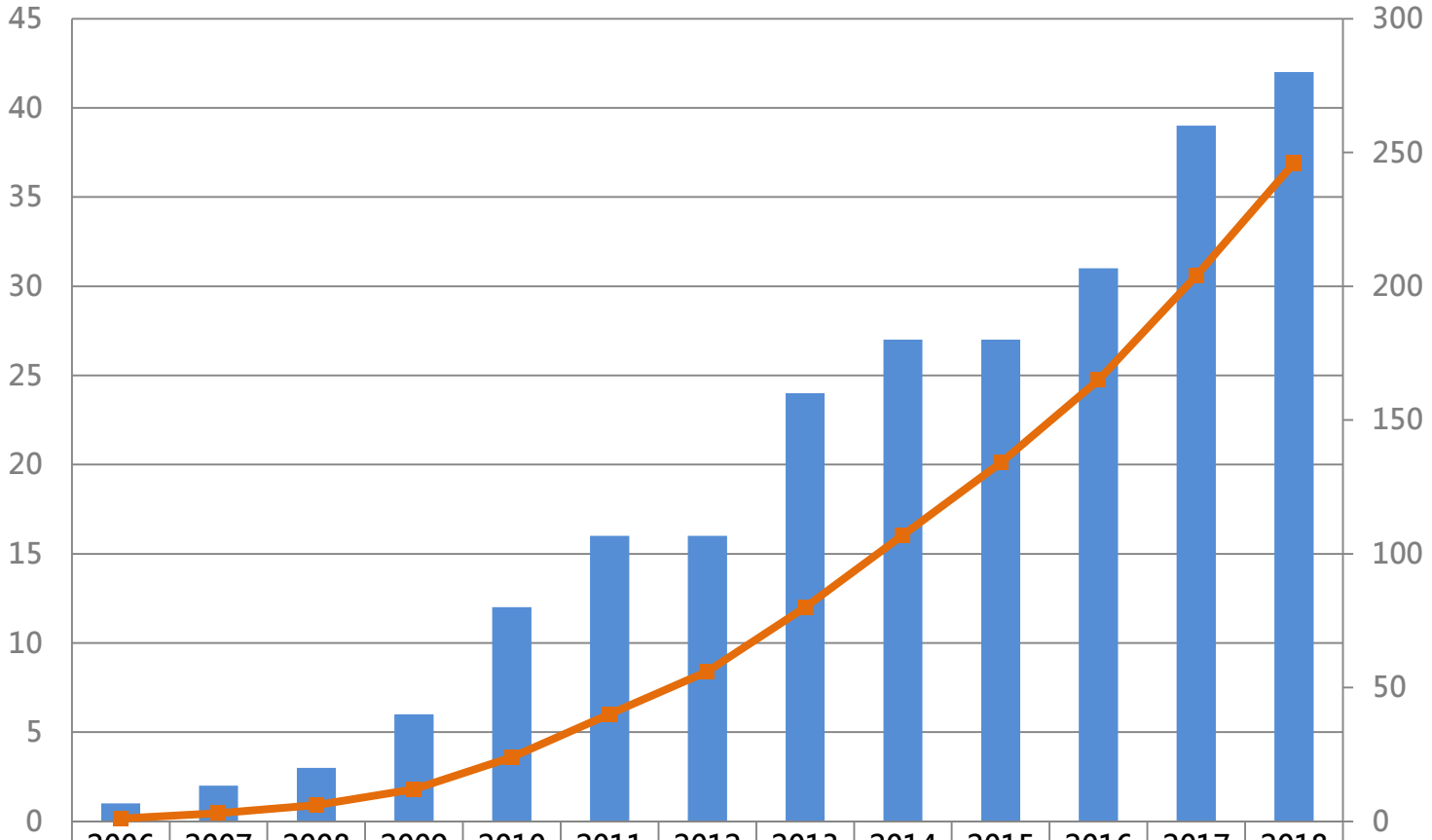


- 生態系統:
  - 合作夥伴超過 130 家



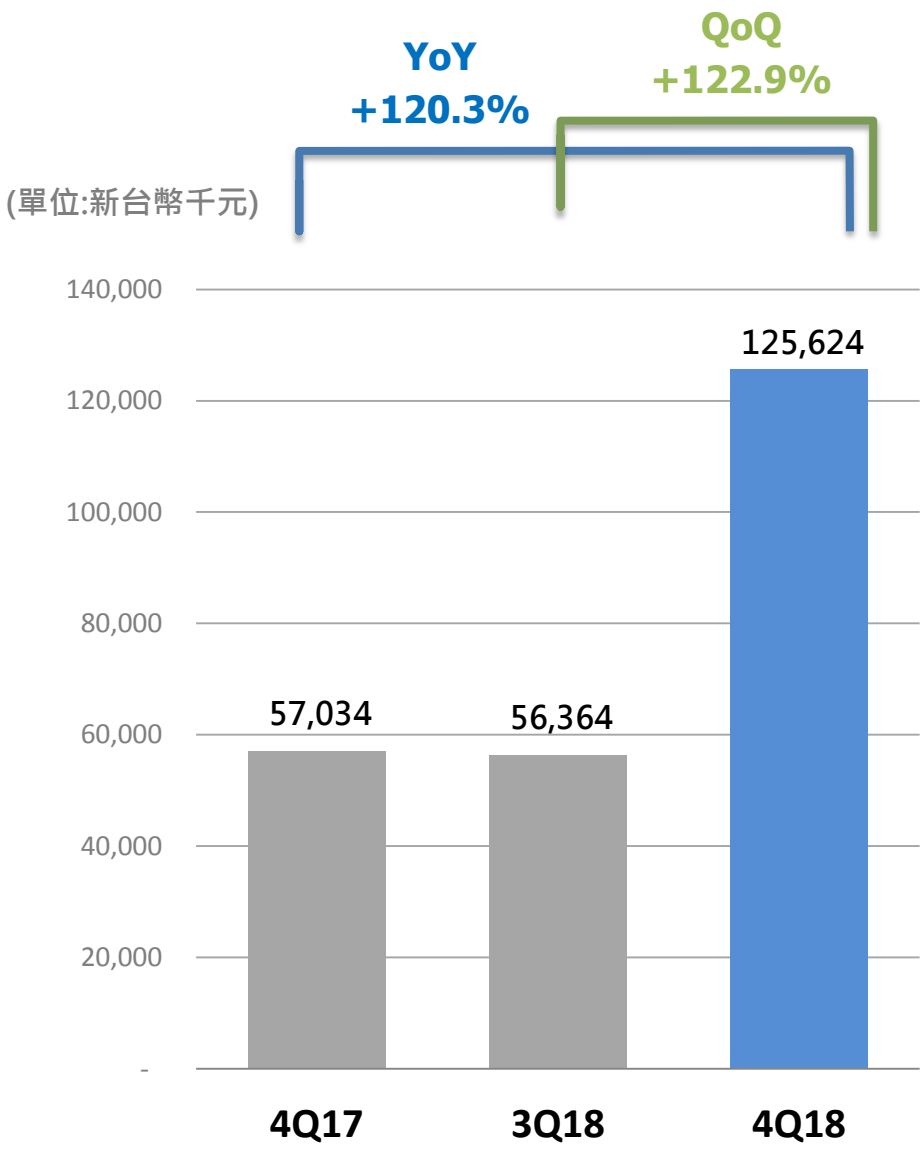
- 嵌入晶心處理器之系統晶片累計出貨量
  - 超過36億顆

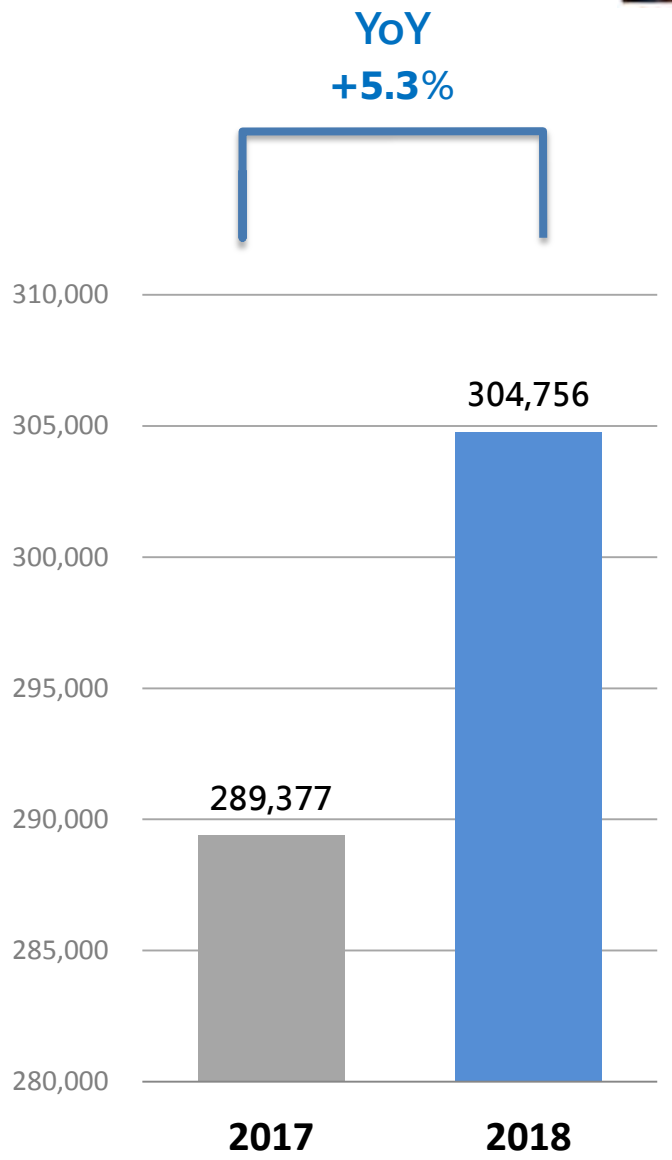
IP 授權合約數穩健成長



	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018
IP授權合約數	1	2	3	6	12	16	16	24	27	27	31	39	42
累計IP授權合約數	1	3	6	12	24	40	56	80	107	134	165	204	246

2018 年度營業收入

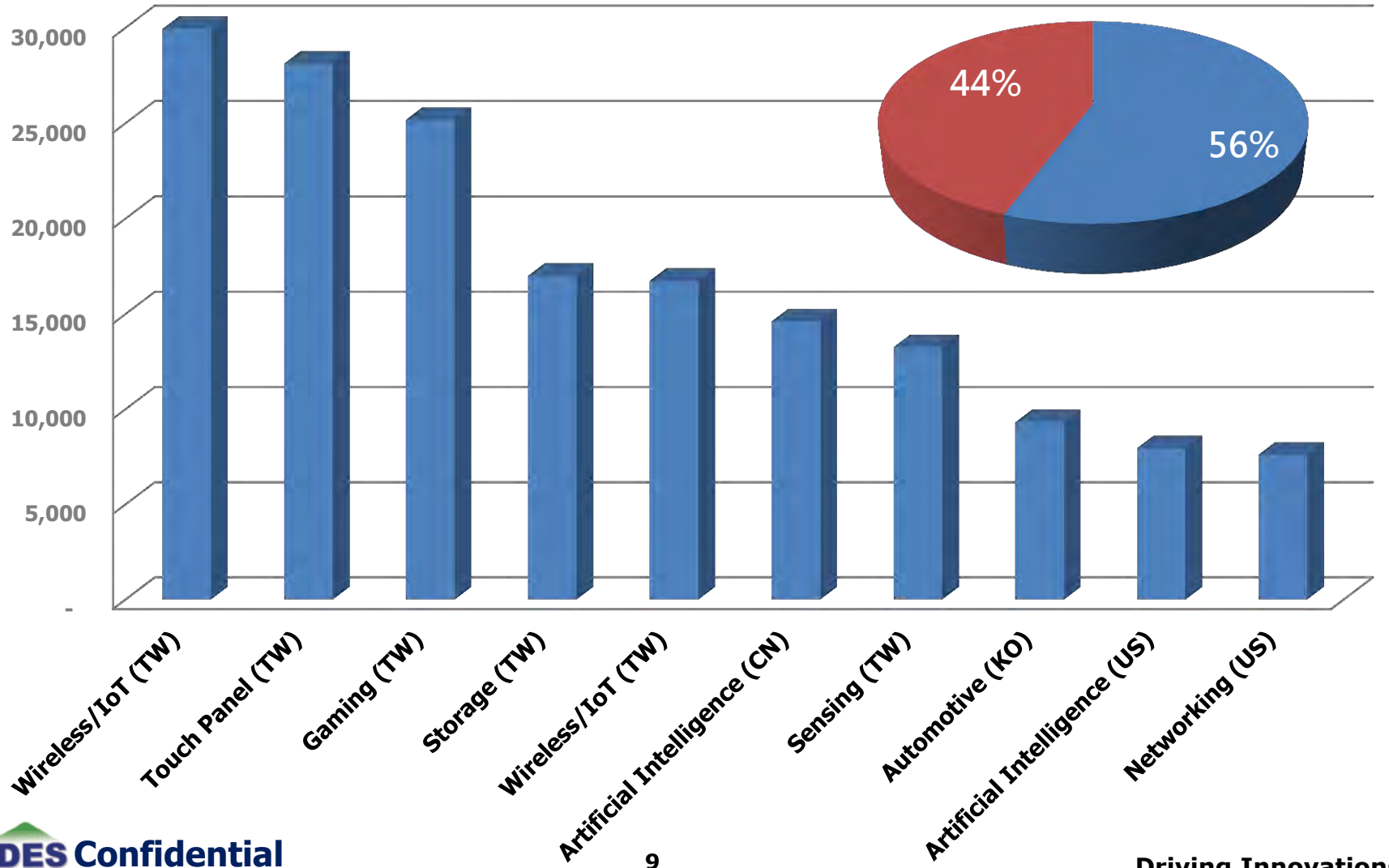

YoY
+120.3%
QoQ
+122.9%
(單位:新台幣千元)
140,000
120,000
100,000
80,000
60,000
40,000
20,000
-
57,034
56,364
125,624
4Q17
3Q18
4Q18


YoY
+5.3%
310,000
305,000
300,000
295,000
290,000
285,000
280,000
289,377
304,756
2017
2018

2018 年前十大客戶之應用分析

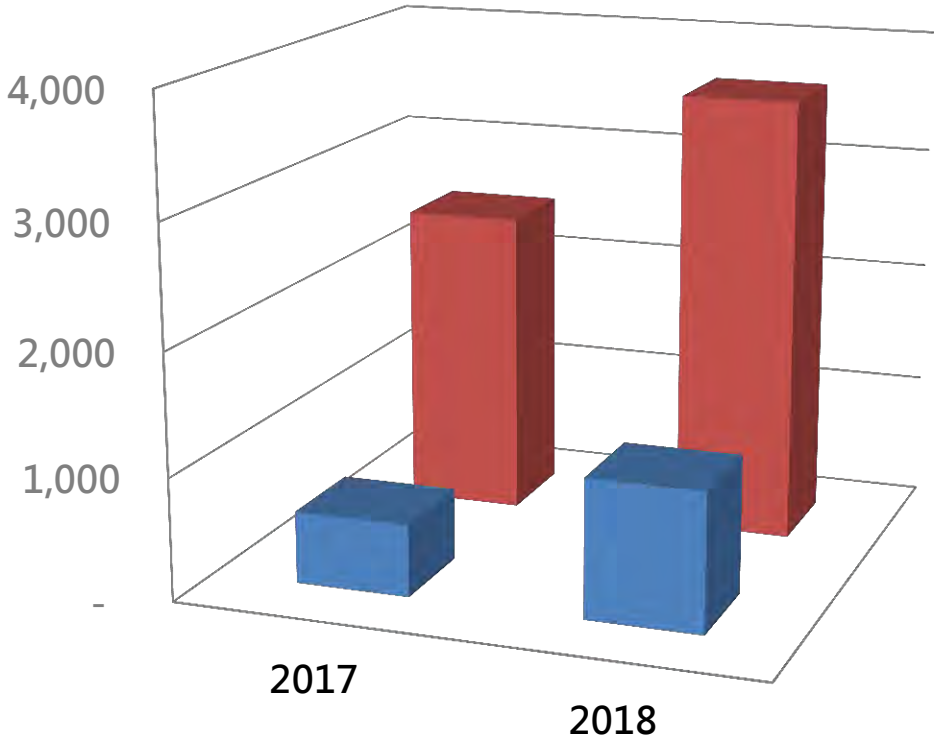
單位: 新台幣千元

前十大客戶貢獻56%的營收



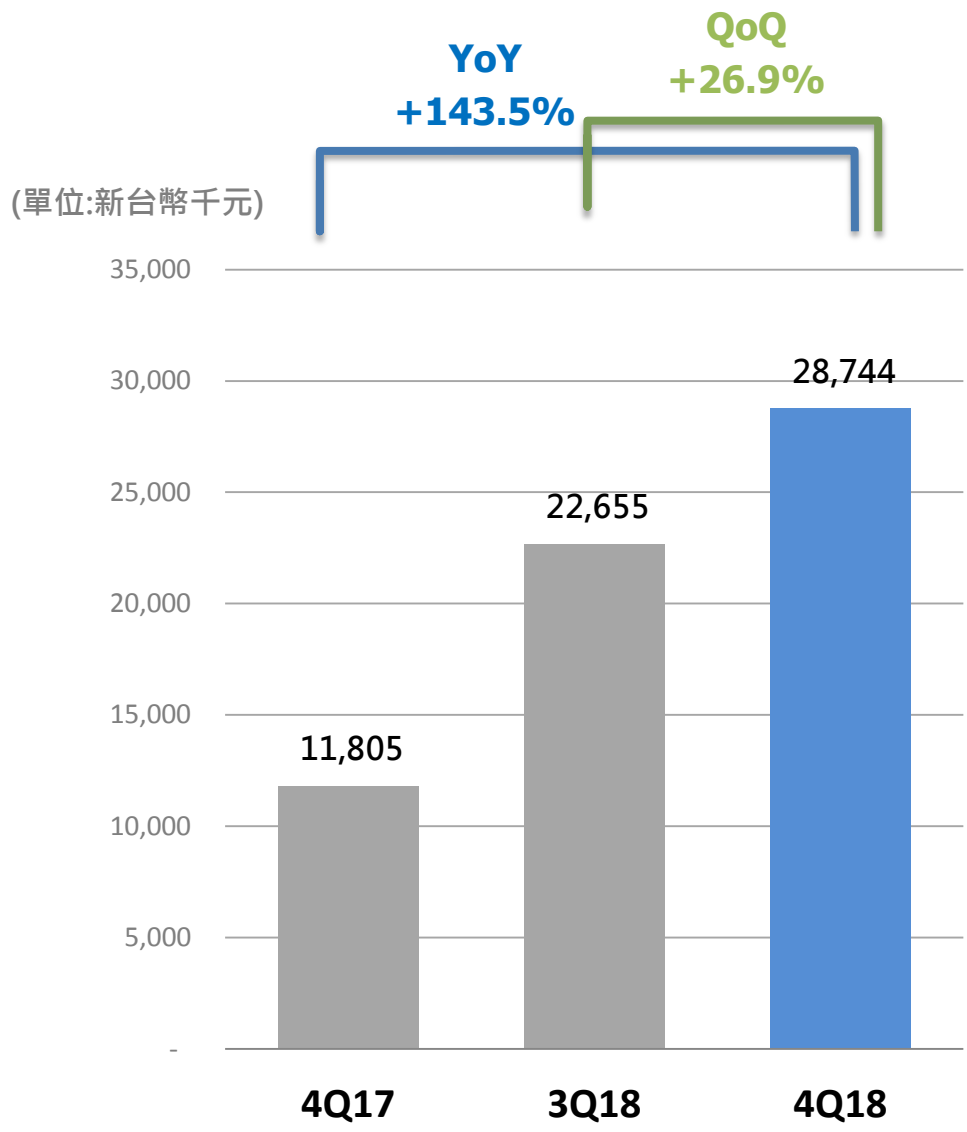
年度及累積 客戶出貨量

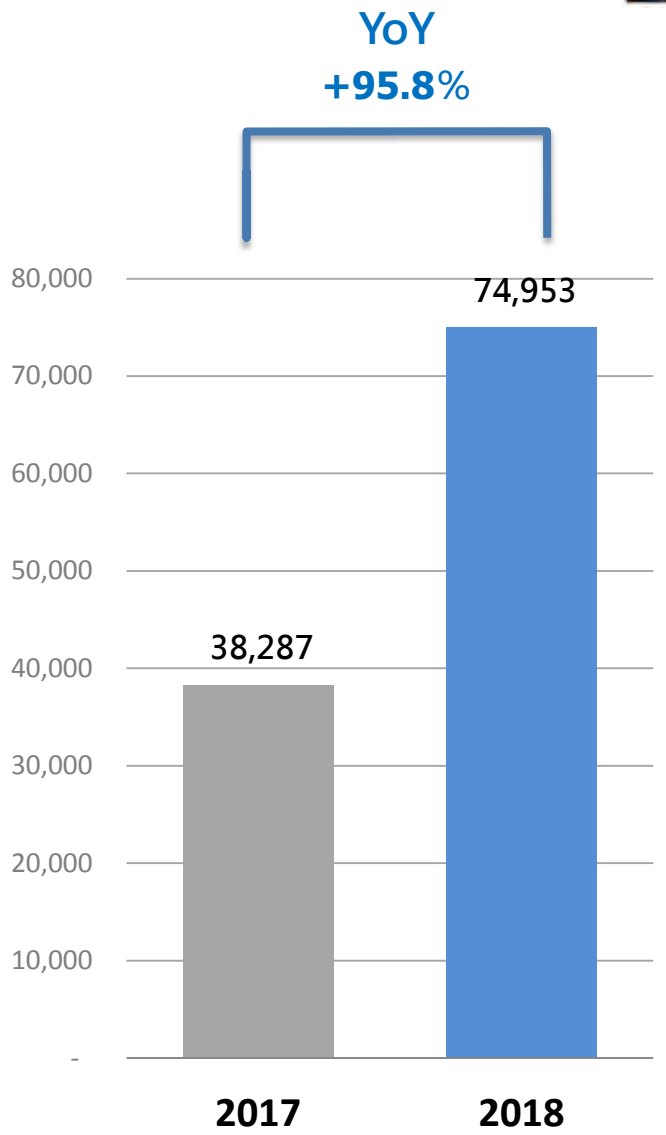
(單位:百萬 顆)



	2017	2018
年度出貨量	590	1,132
累計出貨量	2,500	3,632

2018 年度權利金收入

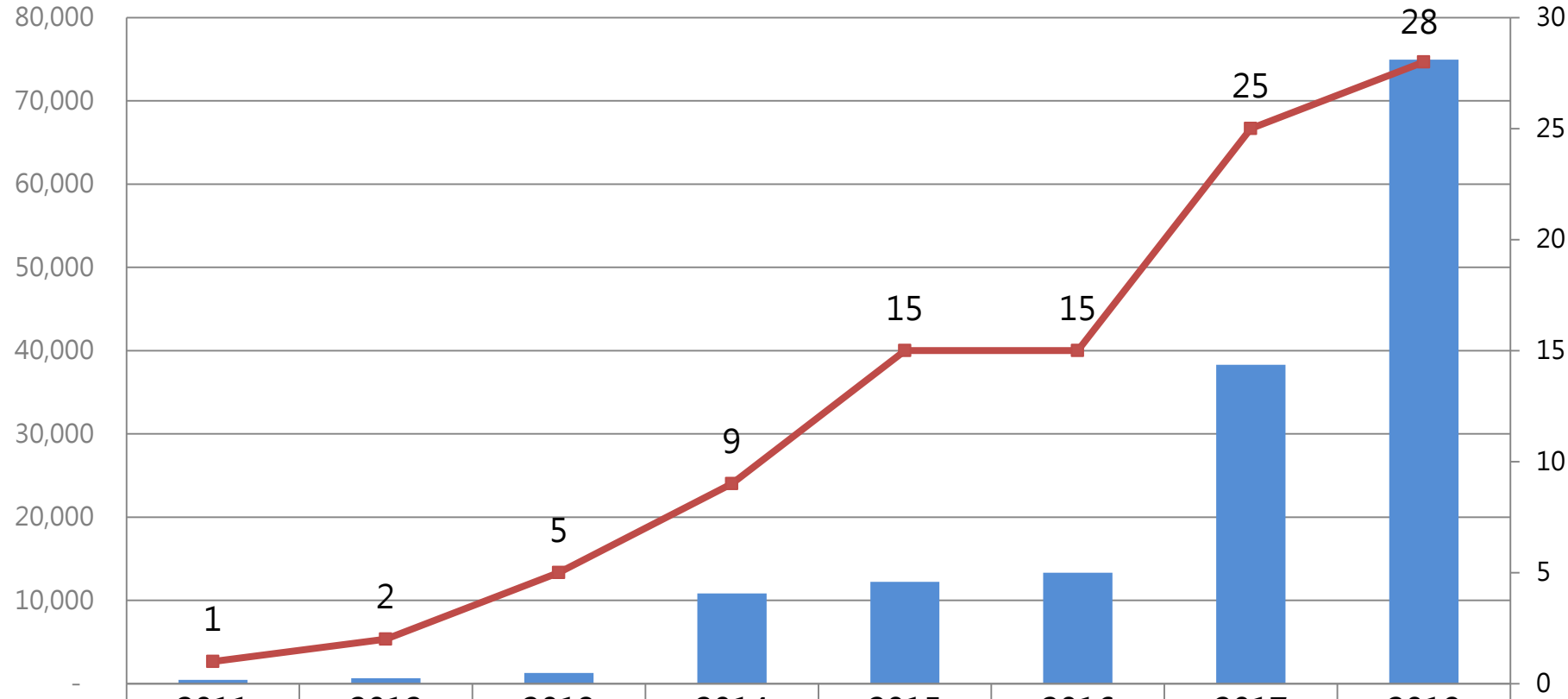




權利金貢獻分析

(單位:新台幣千元)

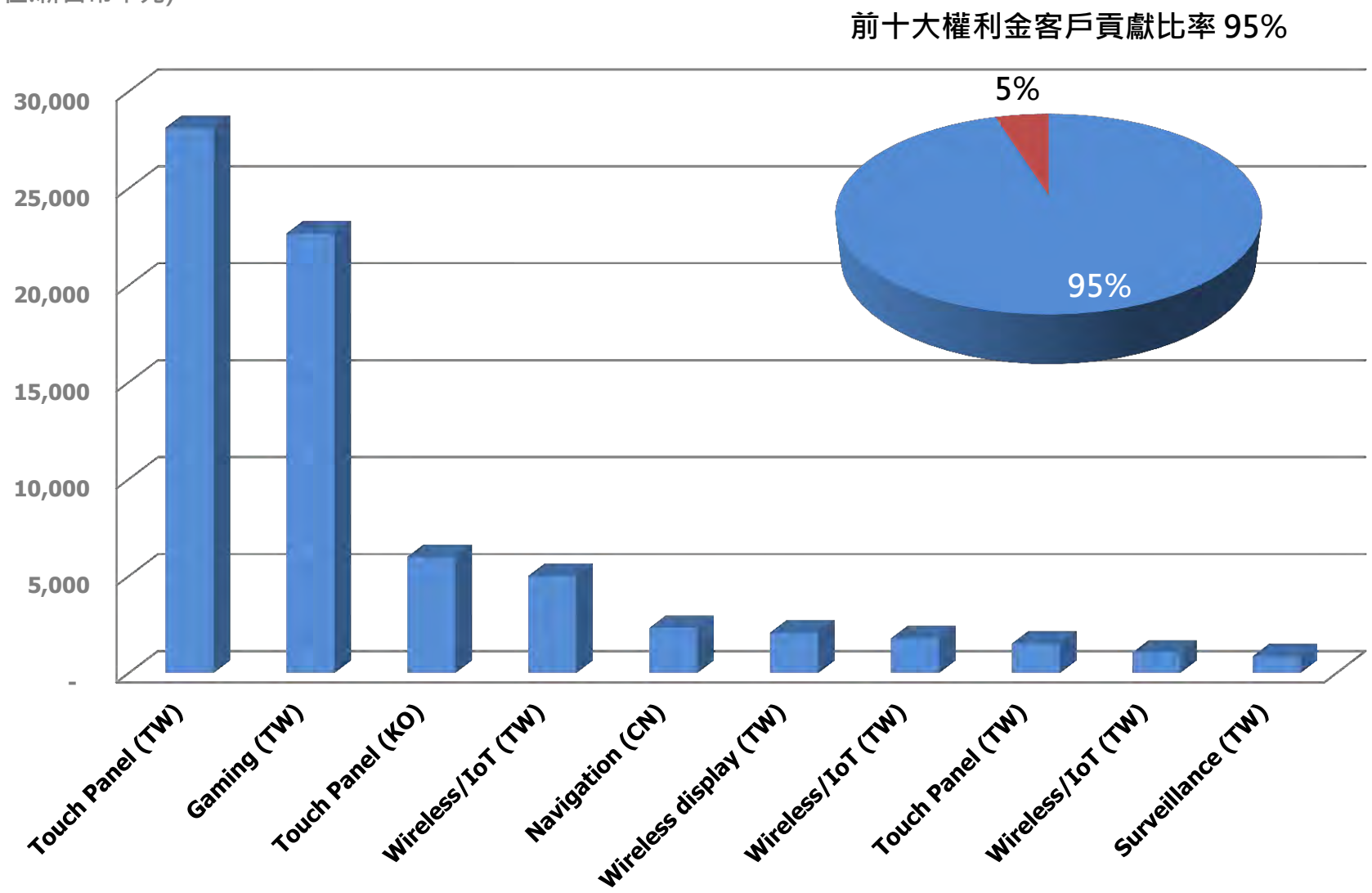
(單位:家數)



	2011	2012	2013	2014	2015	2016	2017	2018
權利金	445	660	1,285	10,819	12,232	13,320	38,287	74,953
客戶數	1	2	5	9	15	15	25	28

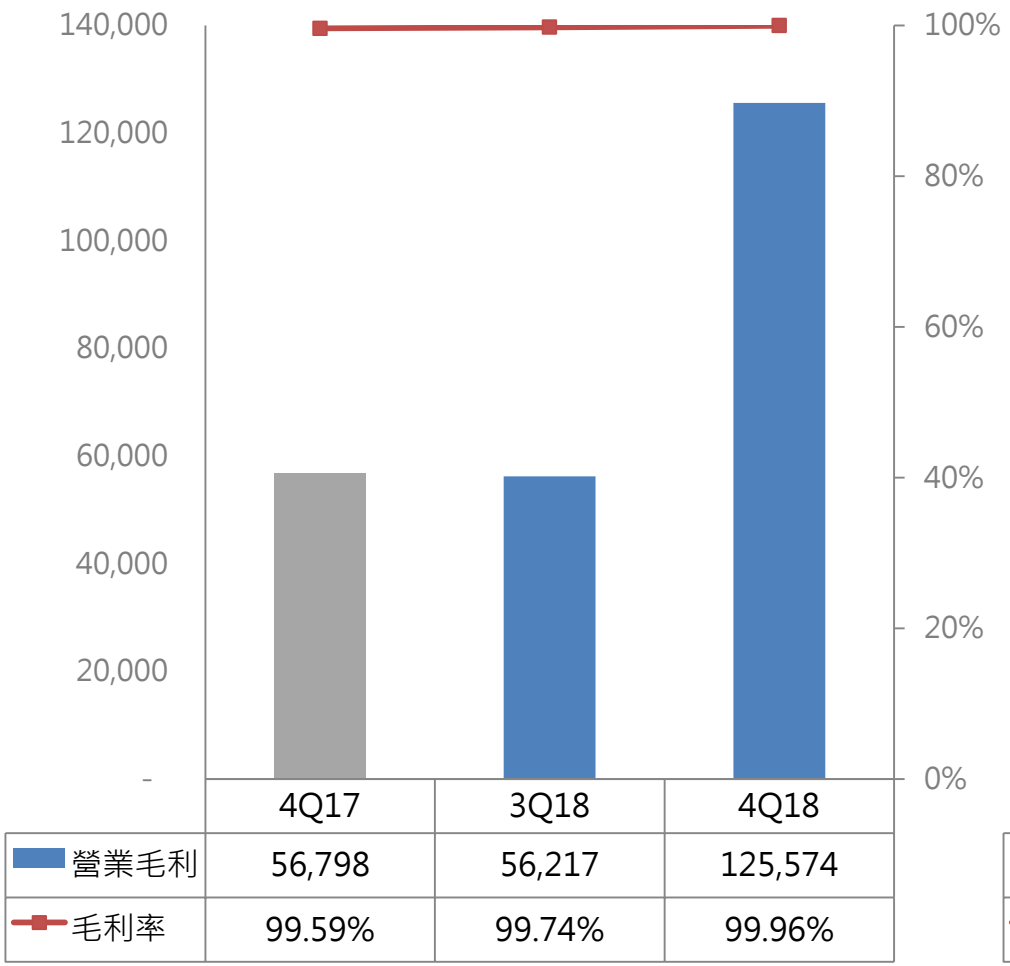
2018 年權利金十大客戶應用分析

(單位:新台幣千元)

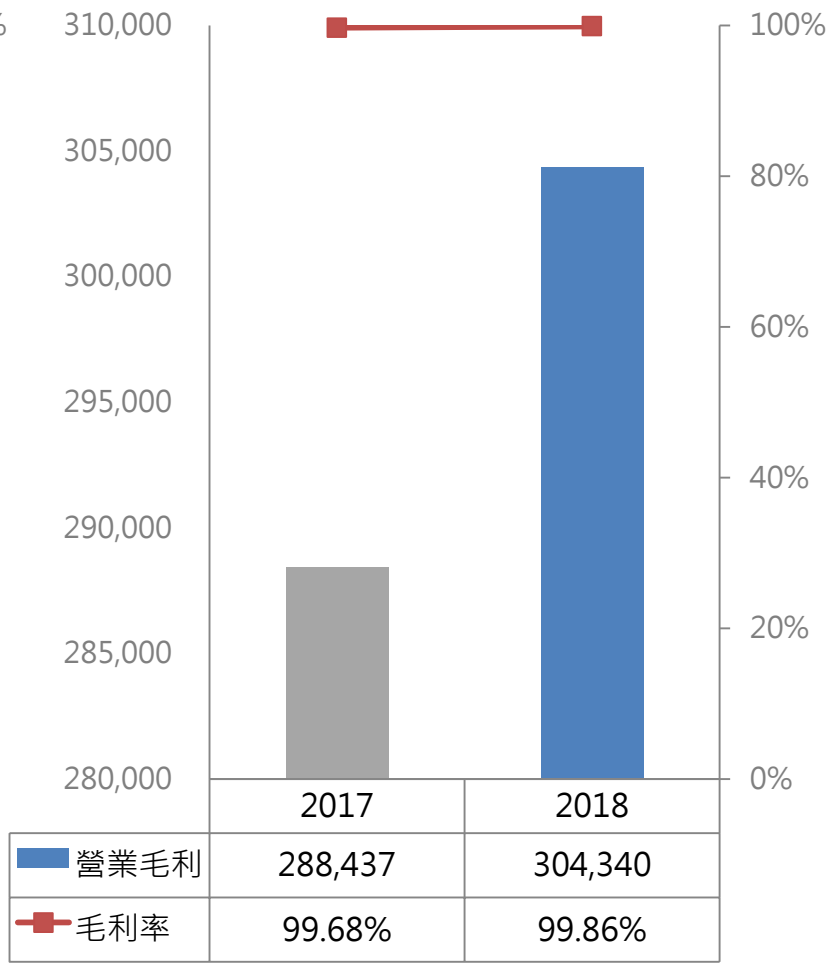


營業毛利與毛利率

(單位:新台幣千元)



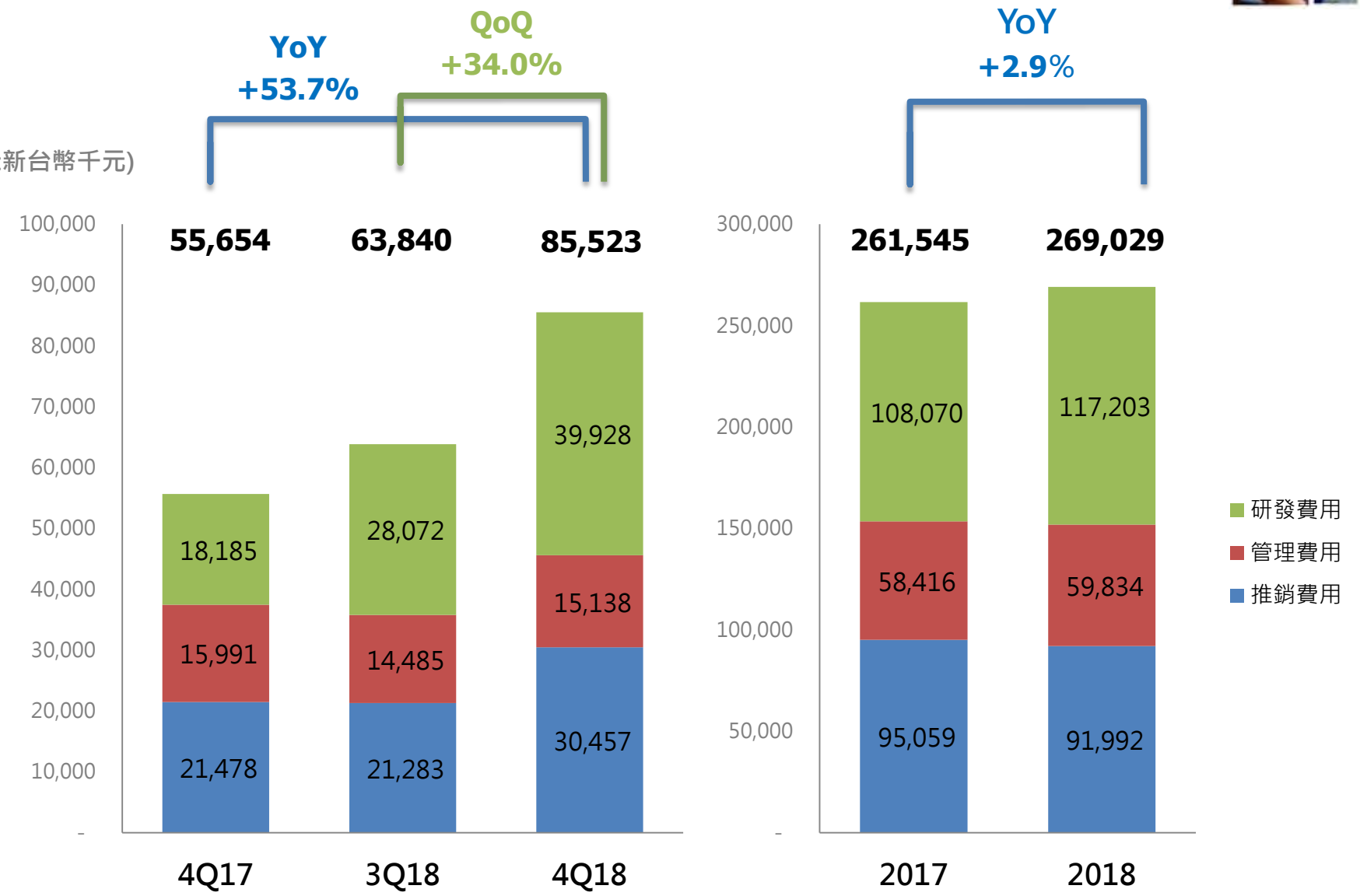
	4Q17	3Q18	4Q18
營業毛利	56,798	56,217	125,574
毛利率	99.59%	99.74%	99.96%



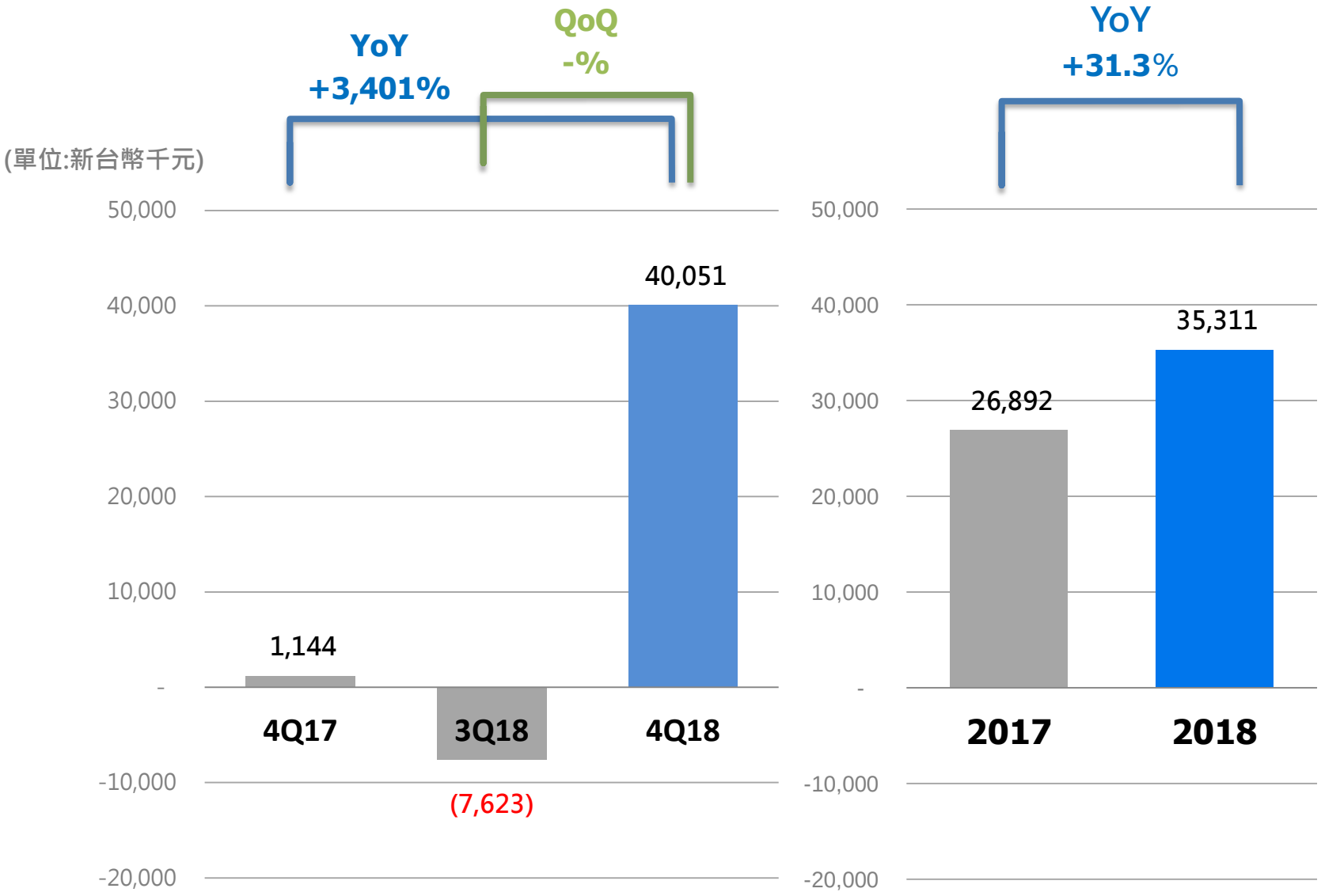
	2017	2018
營業毛利	288,437	304,340
毛利率	99.68%	99.86%

營業費用

(單位:新台幣千元)

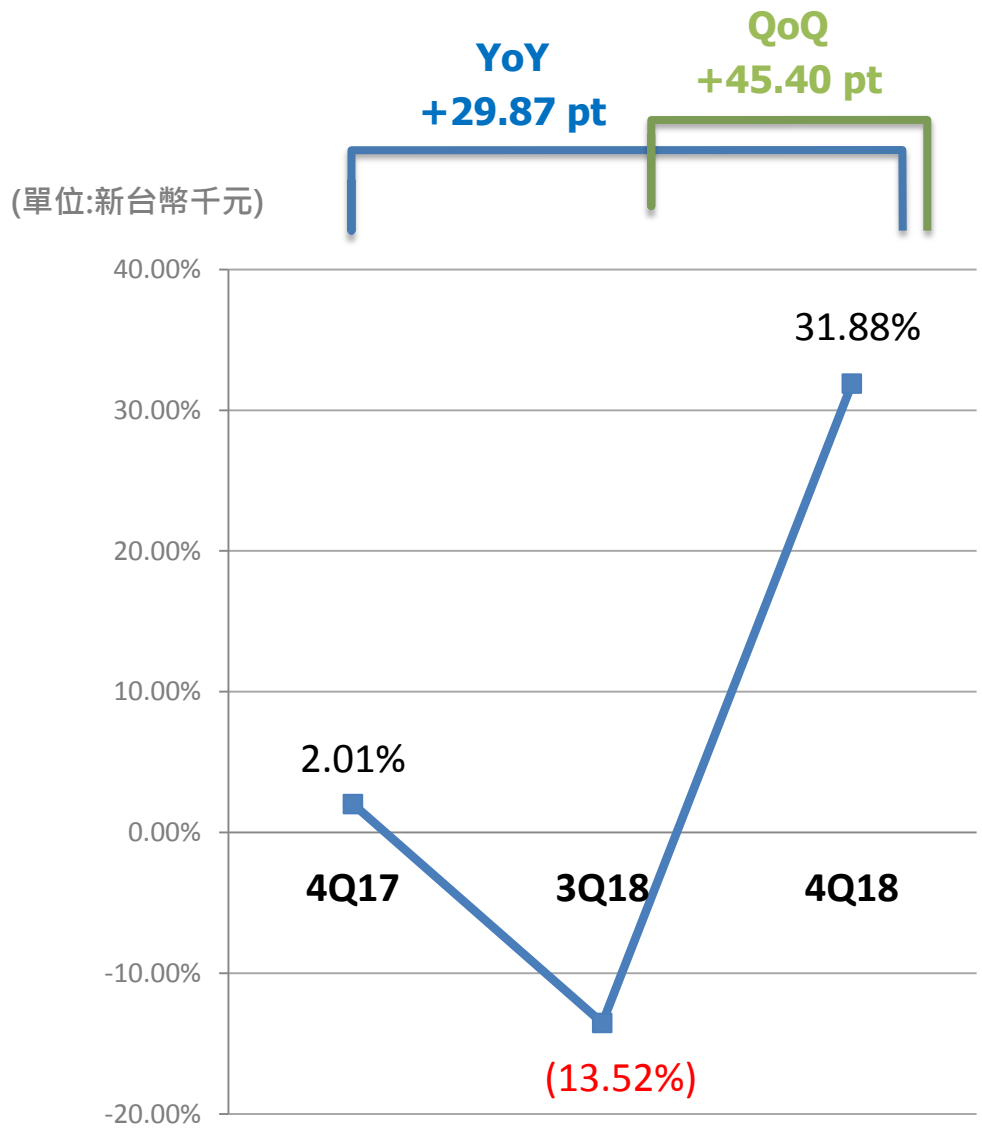


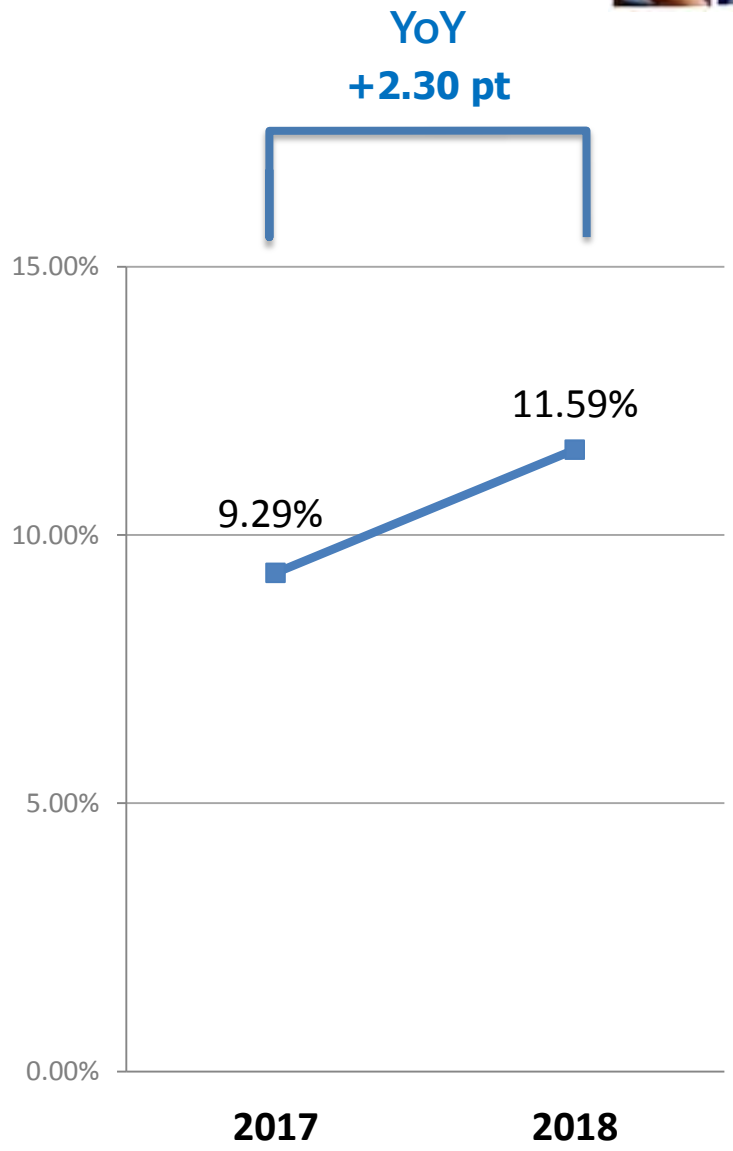
營業利益


YoY
+3,401%
QoQ
-%
(單位:新台幣千元)
50,000
40,000
30,000
20,000
10,000
-
-10,000
-20,000
1,144
40,051
(7,623)
4Q17
3Q18
4Q18
YoY
+31.3%
26,892
35,311
2017
2018

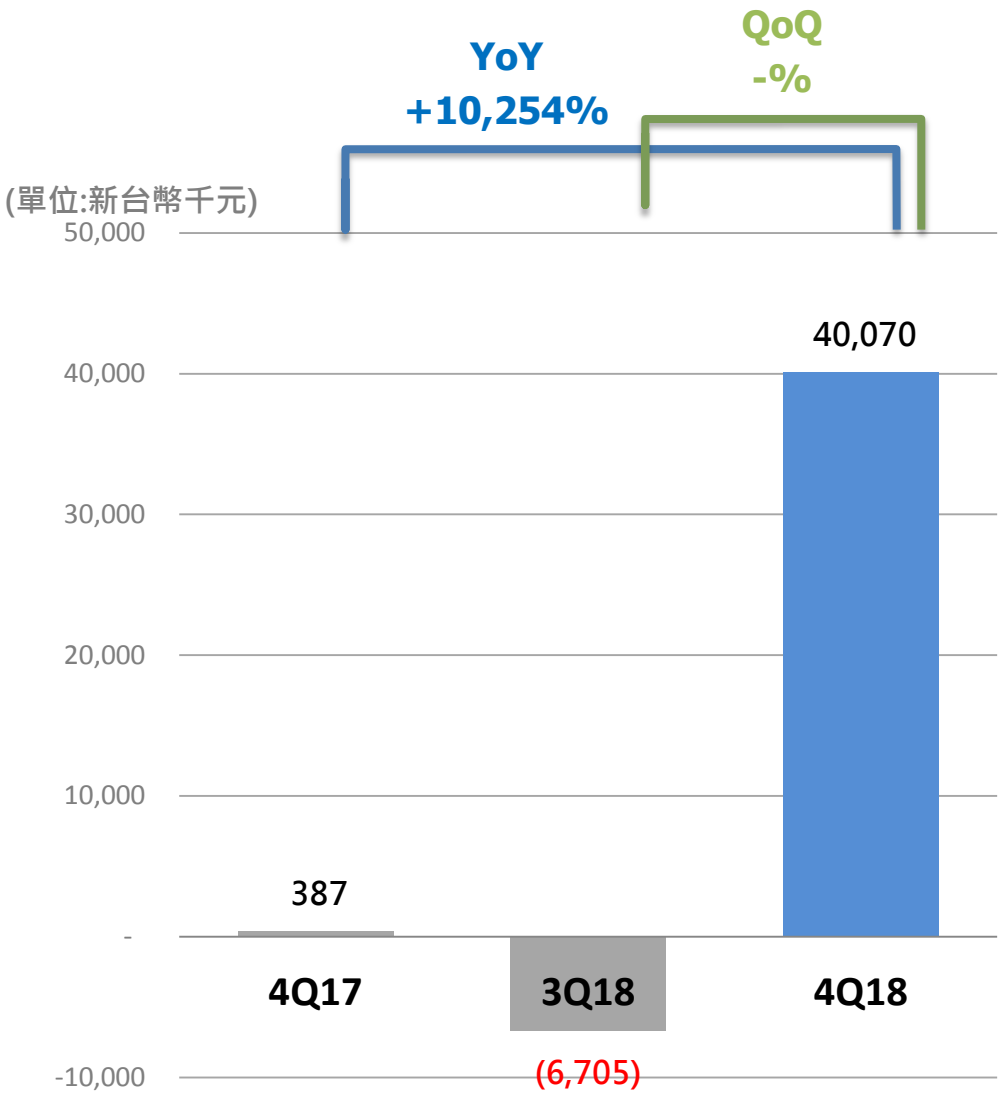
營業利益率

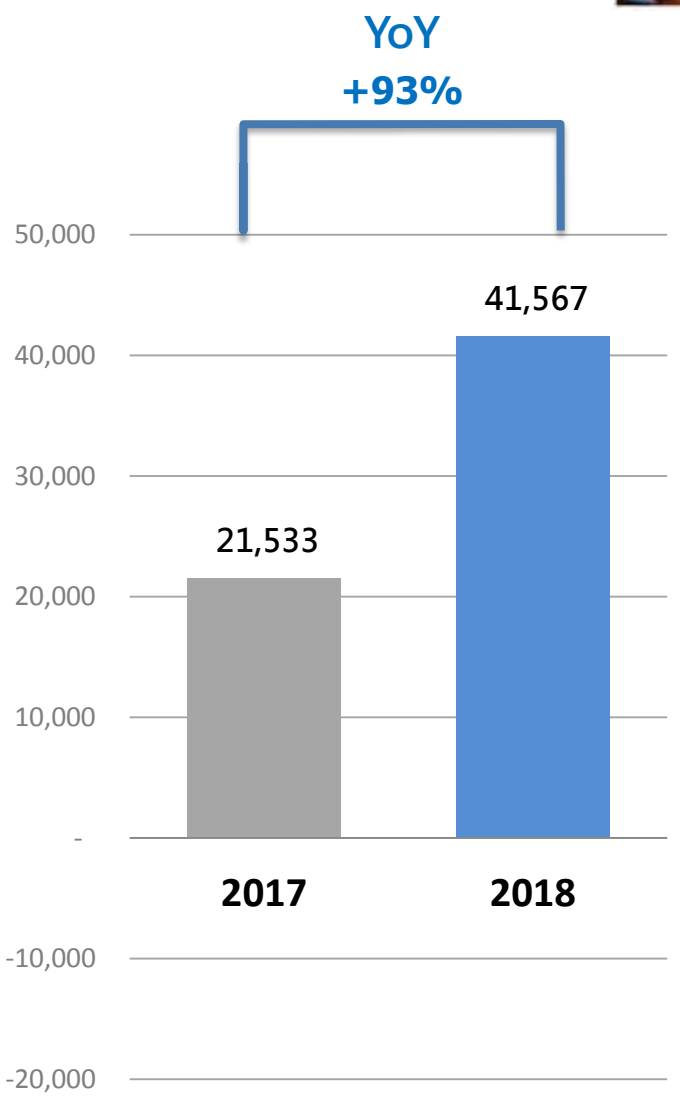
(單位:新台幣千元)





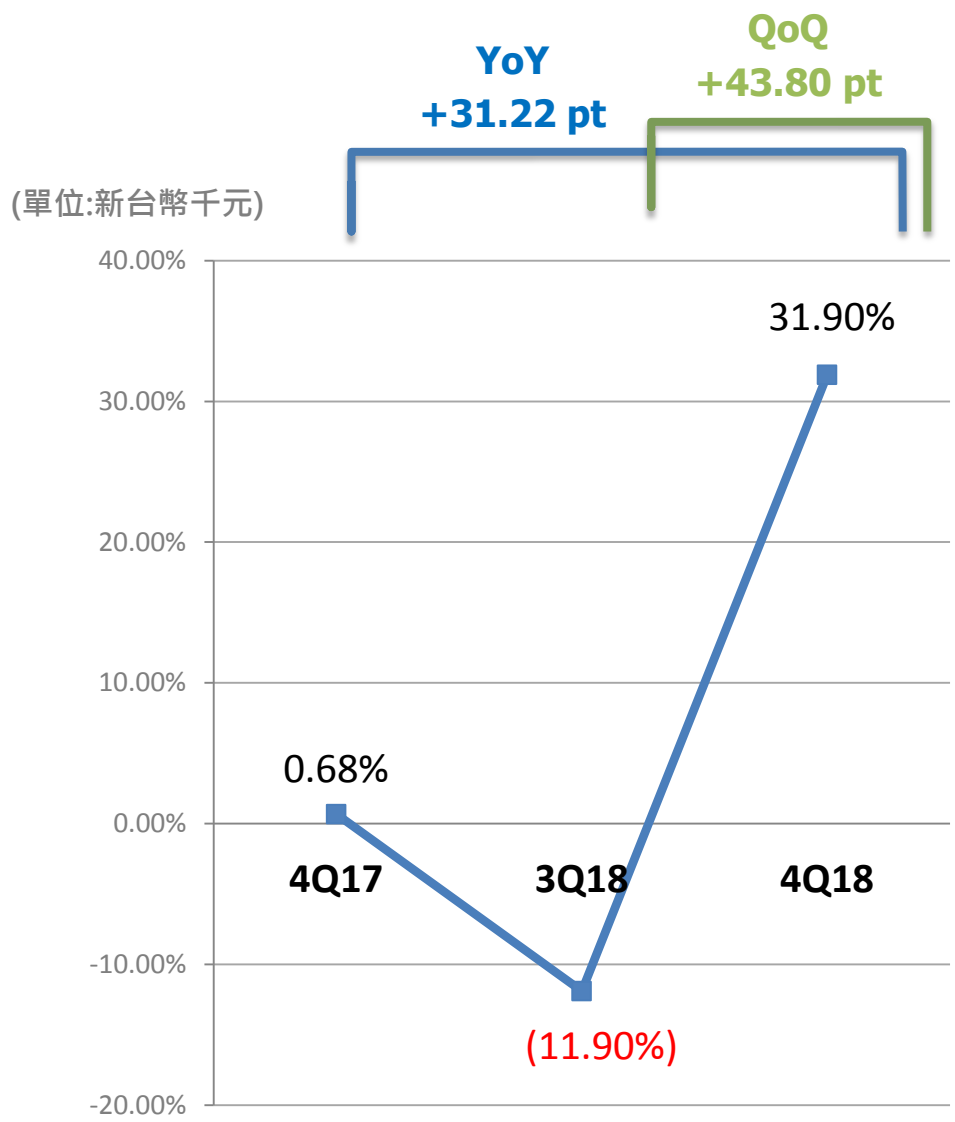
合併淨利

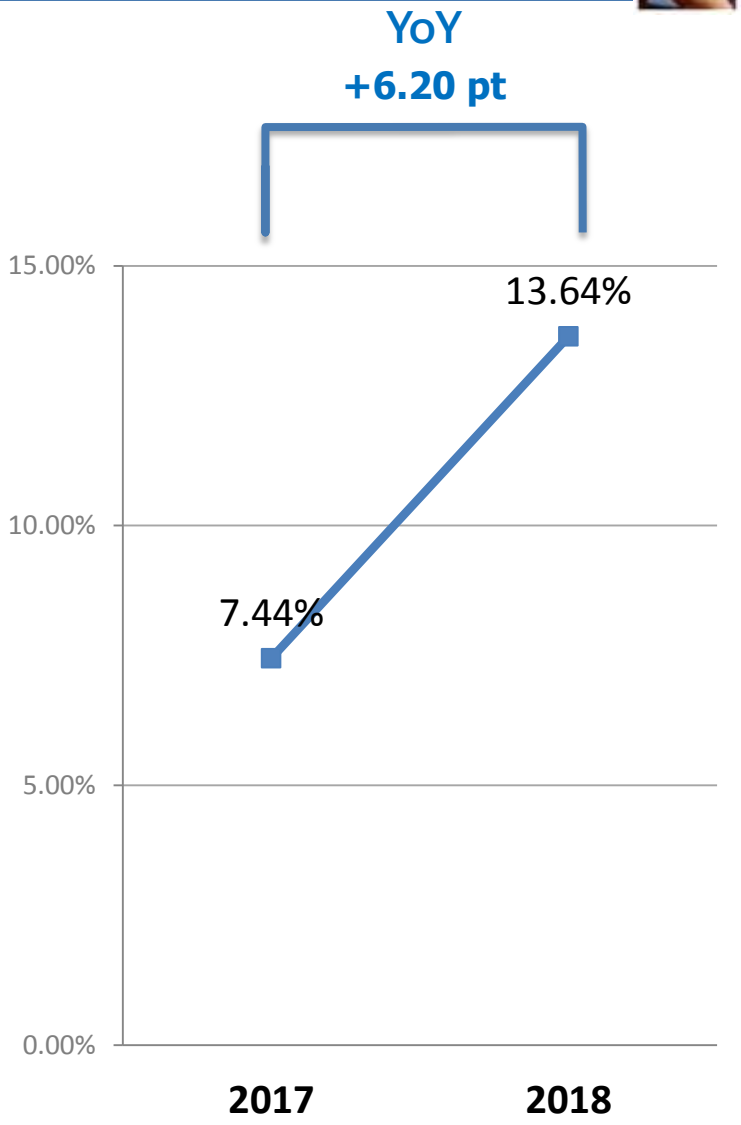

YoY
+10,254%
QoQ
-%
(單位:新台幣千元)
50,000
40,000
30,000
20,000
10,000
-
-10,000
387
40,070
(6,705)
4Q17
3Q18
4Q18


YoY
+93%
50,000
40,000
30,000
20,000
10,000
-
-10,000
-20,000
21,533
41,567
2017
2018

合併淨利率

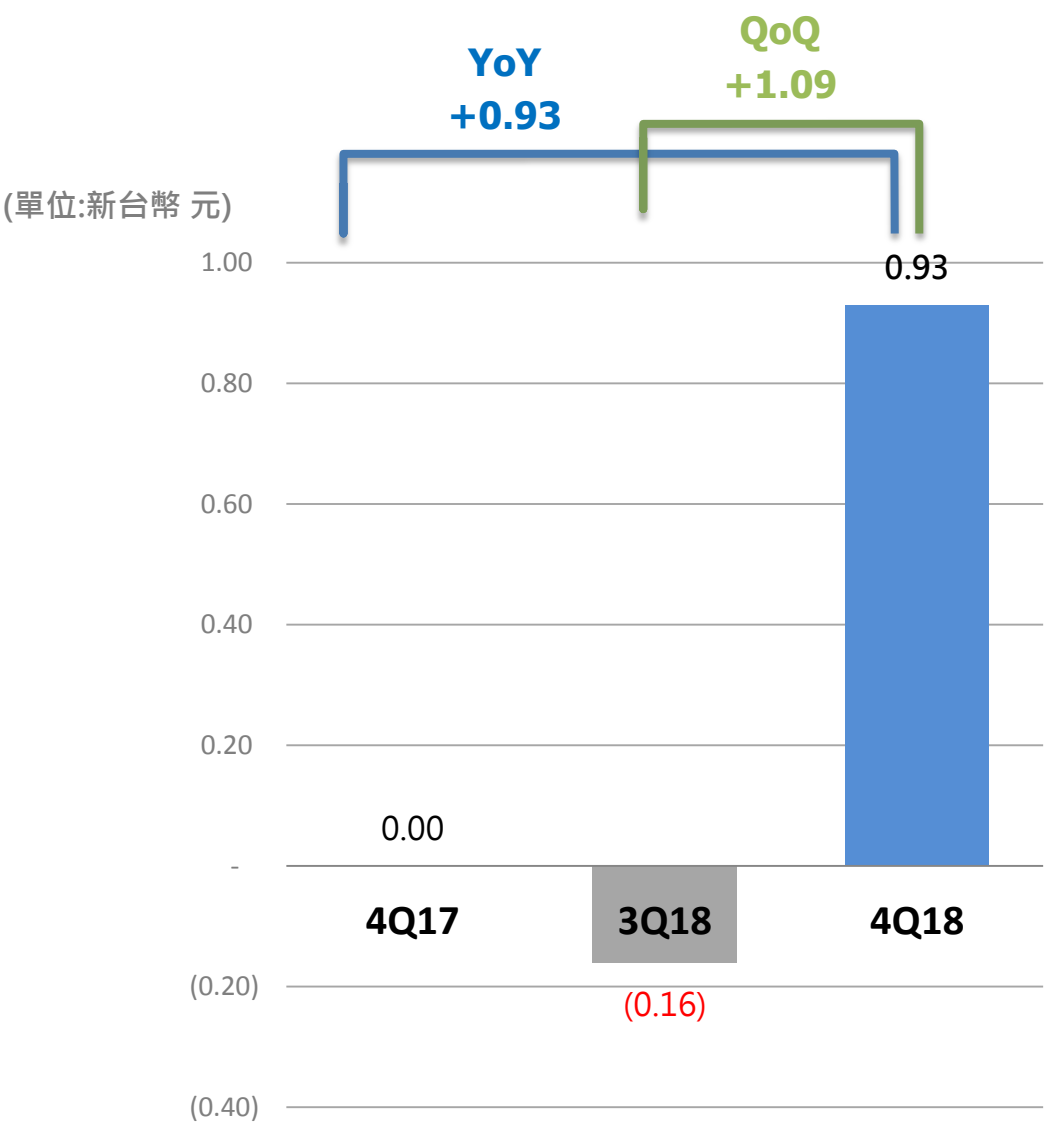
(單位:新台幣千元)

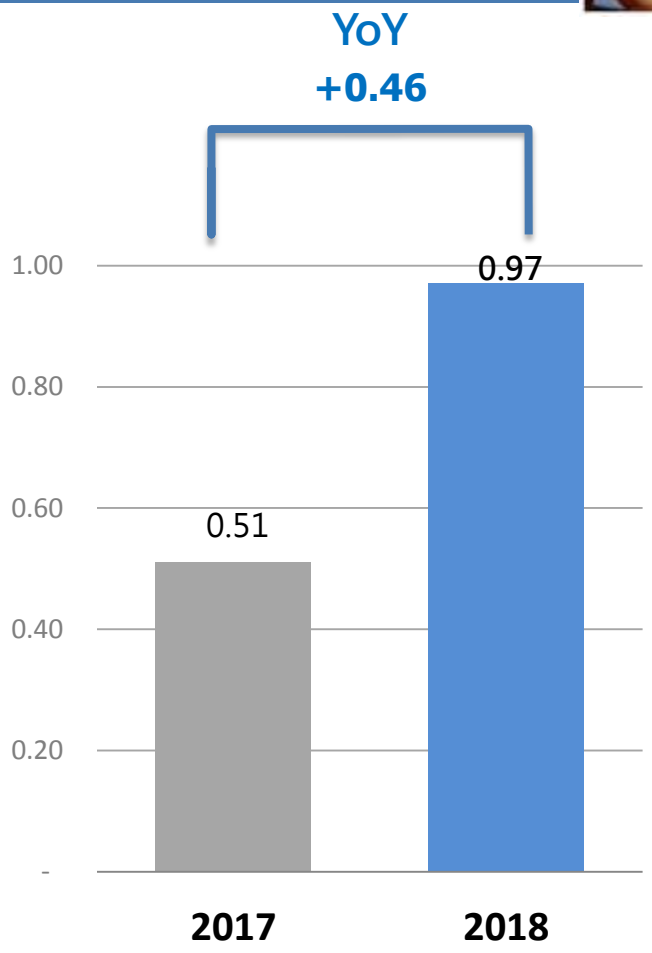




每股盈餘

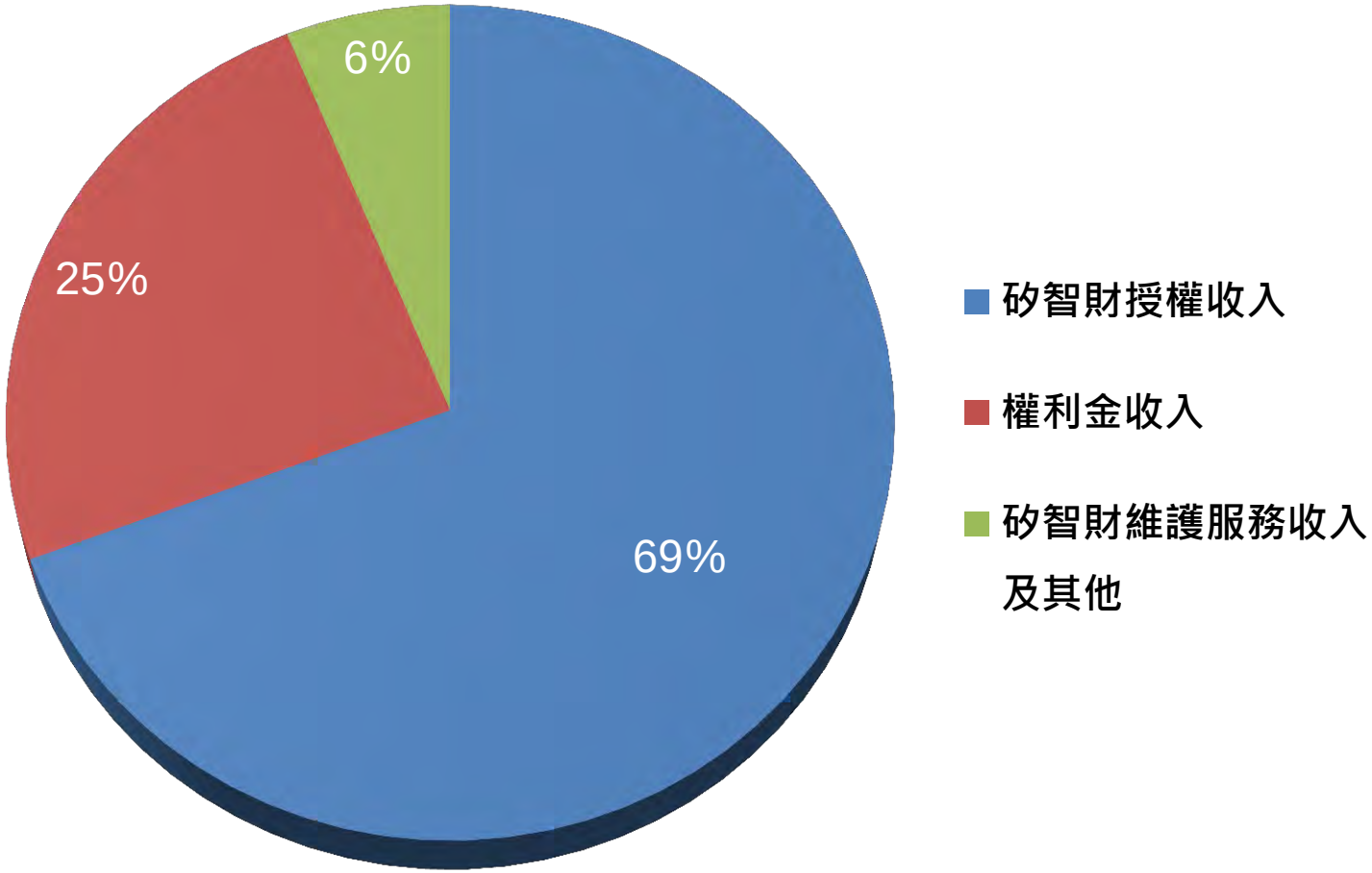
(單位:新台幣 元)


YoY
+0.93
QoQ
+1.09
1.00
0.80
0.60
0.40
0.20
-
(0.20)
(0.40)
0.00
0.93
(0.16)
4Q17
3Q18
4Q18

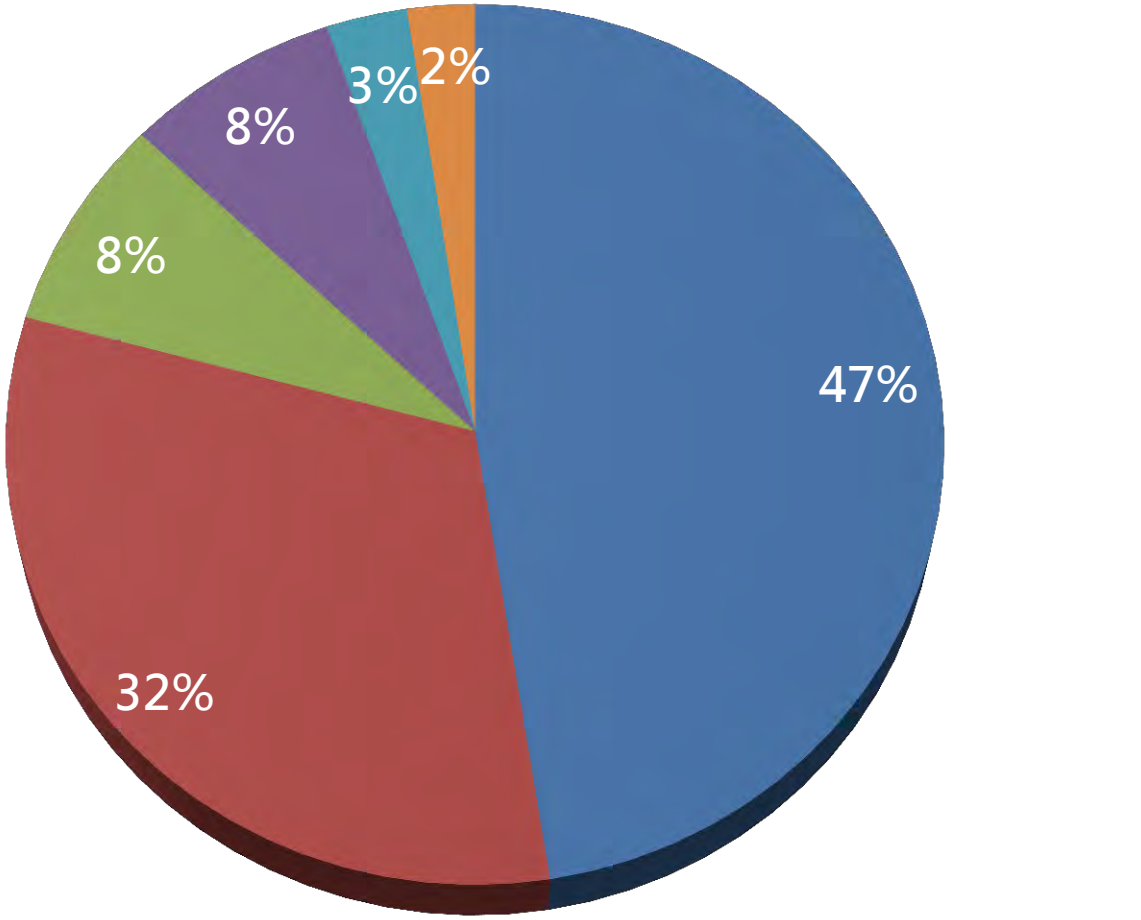

YoY
+0.46
1.00
0.80
0.60
0.40
0.20
-
0.51
0.97
2017
2018

2018 年度銷售分析-收入模式

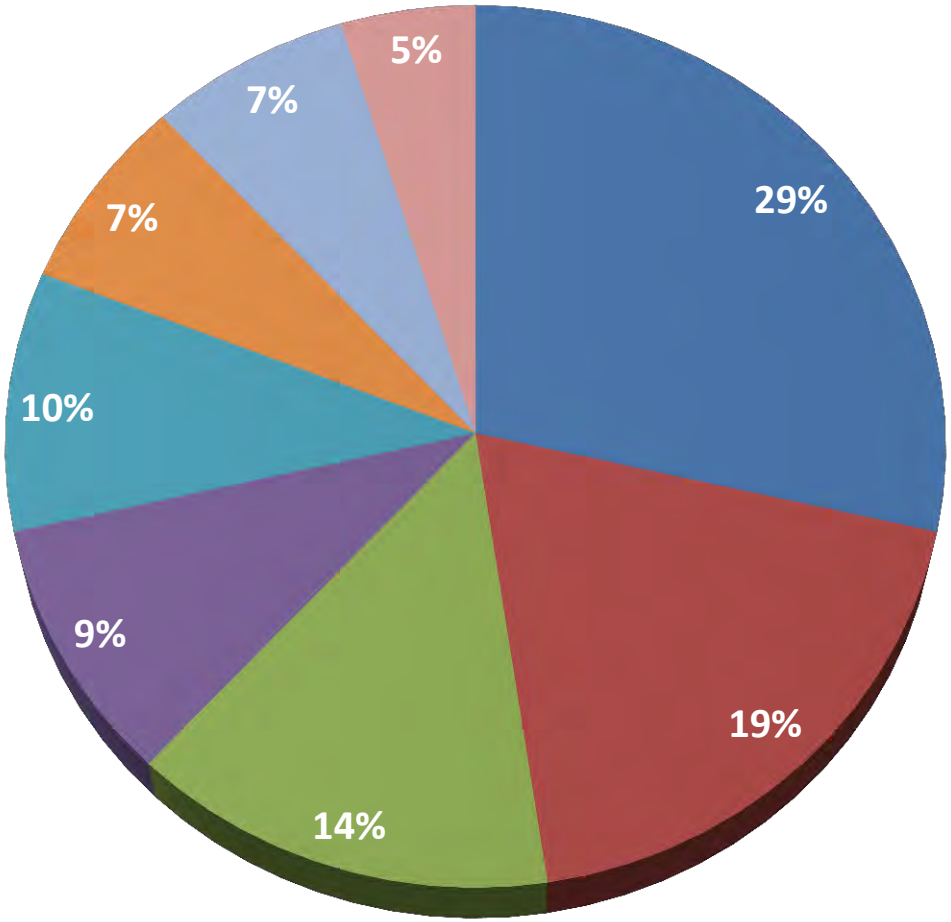
(2018/01-12 新合約數: 42)



2018 年度銷售分析-地區別

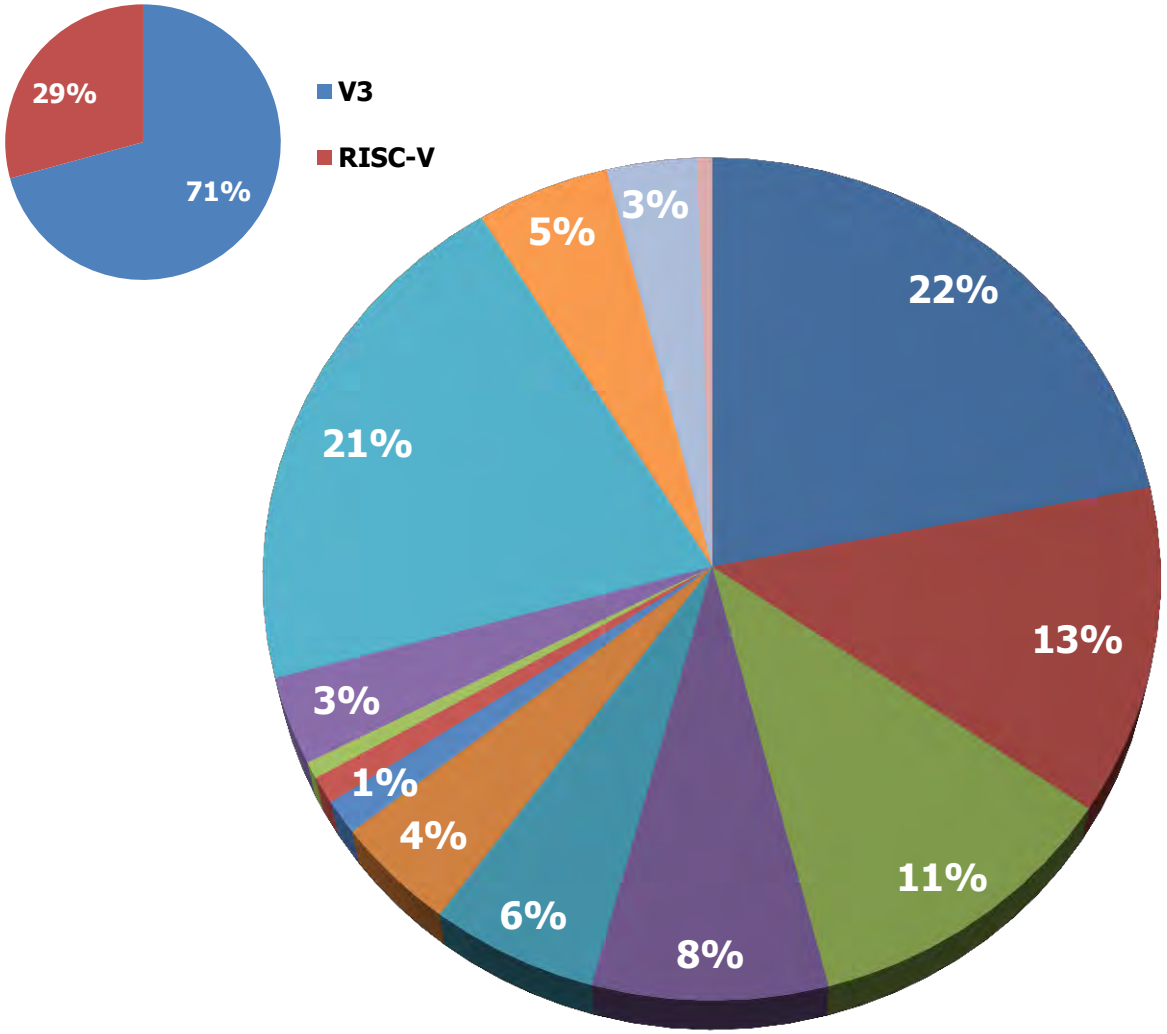


2018 年度銷售分析-客戶應用



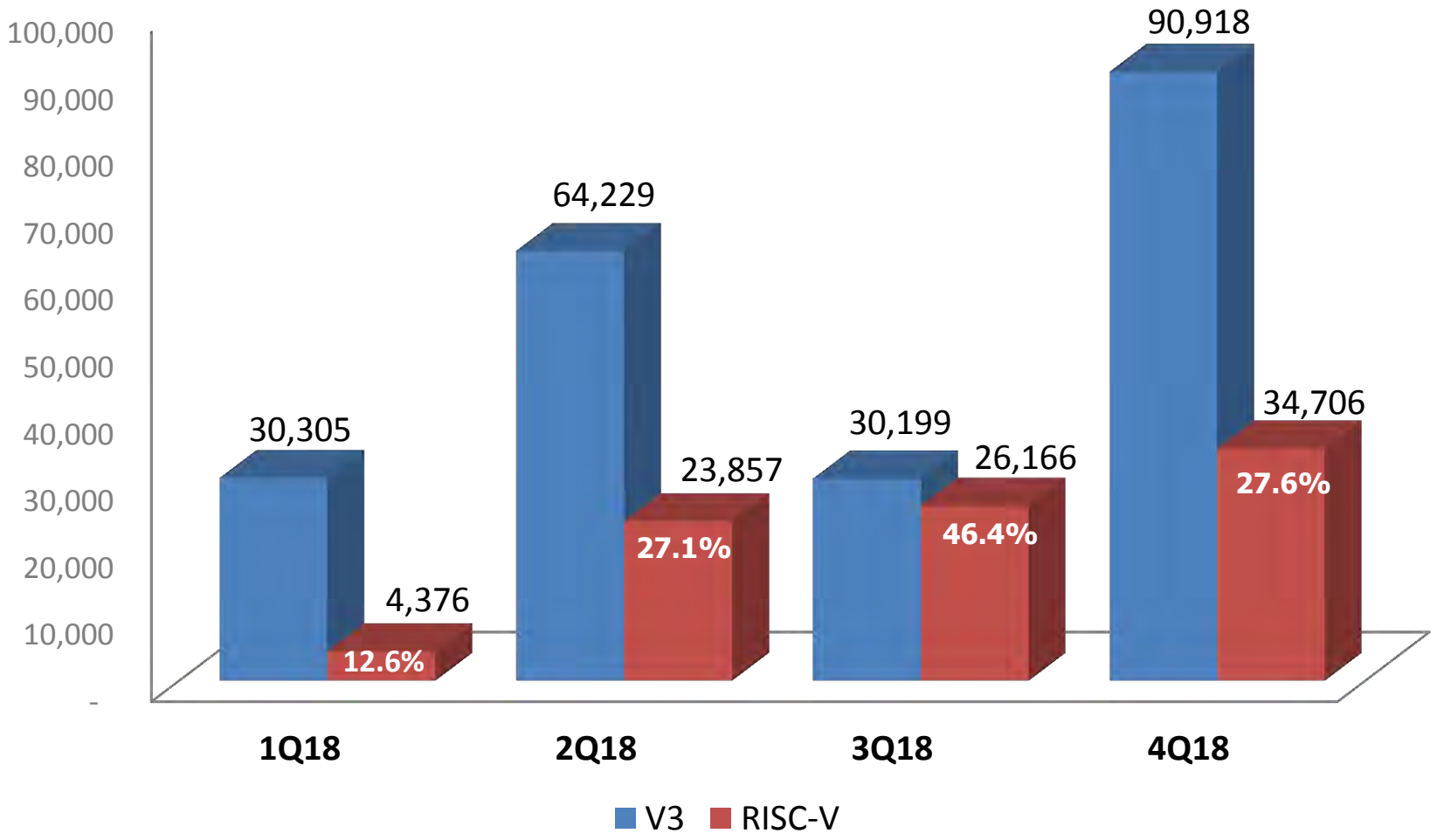
*Based on agreement number

2018 年度銷售分析-產品別



2018 年度銷售分析- RISC-V

(單位:新台幣千元)

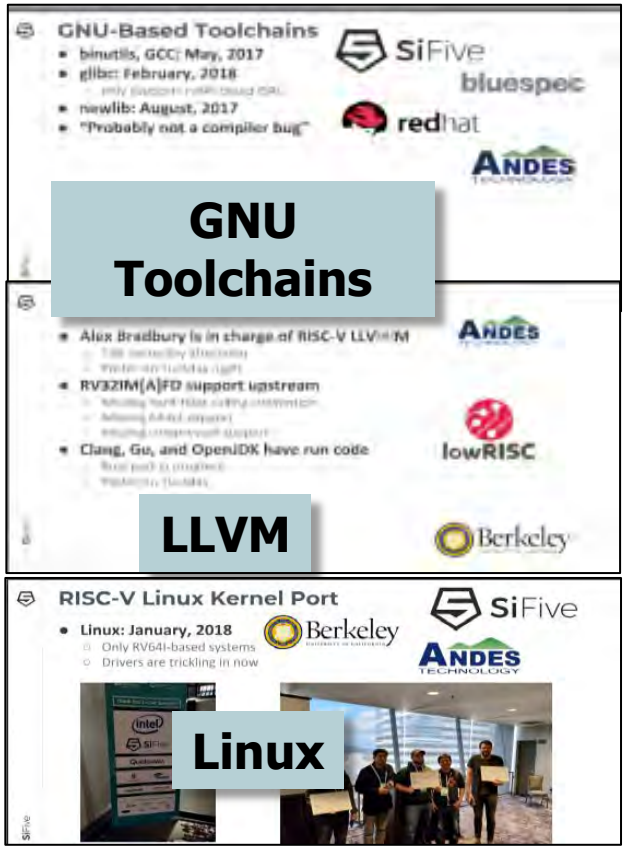


產品應用

晶心概況

- A 14-year-old public CPU IP company
- >1B Andes-Embedded SoC shipped in 2018. >3.6B cumulatively.

- A founding member of the RISC-V Foundation
- A major open source maintainer/contributor
- Active involvement in standard extensions
  - Chair of P-extension (Packed DSP/SIMD) Task Group
  - Co-chair of Fast Interrupt Task Group



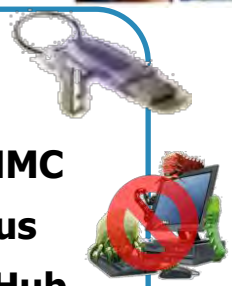
豐富多樣的客戶應用

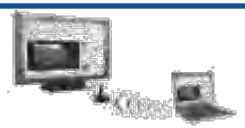
- Touch Screen
- eBook/eDictionary
- Power management
- Bio-medical device
- CMMB
- MCU
- TCON

Consumer

Storage & Sensor

- USB3.0
- SSD, eMMC
- Anti-virus
- Sensor Hub
- mSATA
- Secure SD
- Fingerprint Recognition





- Wireless display
- WiFi, Bluetooth
- GPS, GPON, NFC
- Gateway/router
- Portable Karaoke
- Sigfox LPWAN
- IoT Cat0 base station
- IoT MCU • ESL
- Smart Meter • Smart Lighting

Communication & IoT

Industrial & Video

- Motor Control
- Wireless Charger
- Surveillance
- Barcode scanner
- ADAS
- VEDR
- 4K2K CODEC
- 8K4K CODEC

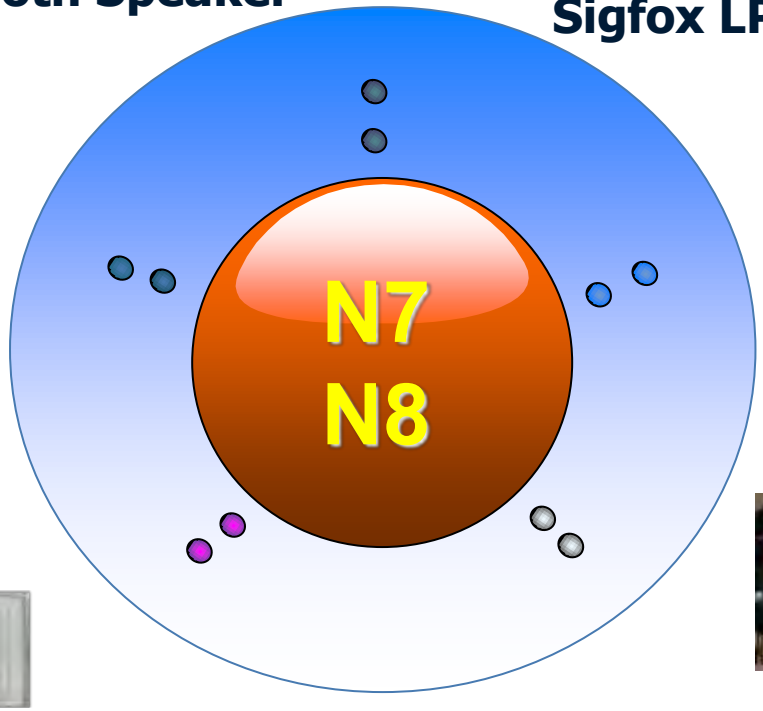
and more.....

物聯網應用 - 1

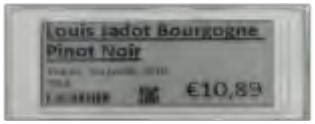
Bluetooth Speaker

Sigfox LPWAN

Healthcare device



Wearable device



Electronic price tags

Sensor Hub

物聯網應用 - 2

Wearable devices

Drone

Portable Karaoke

N9
D10

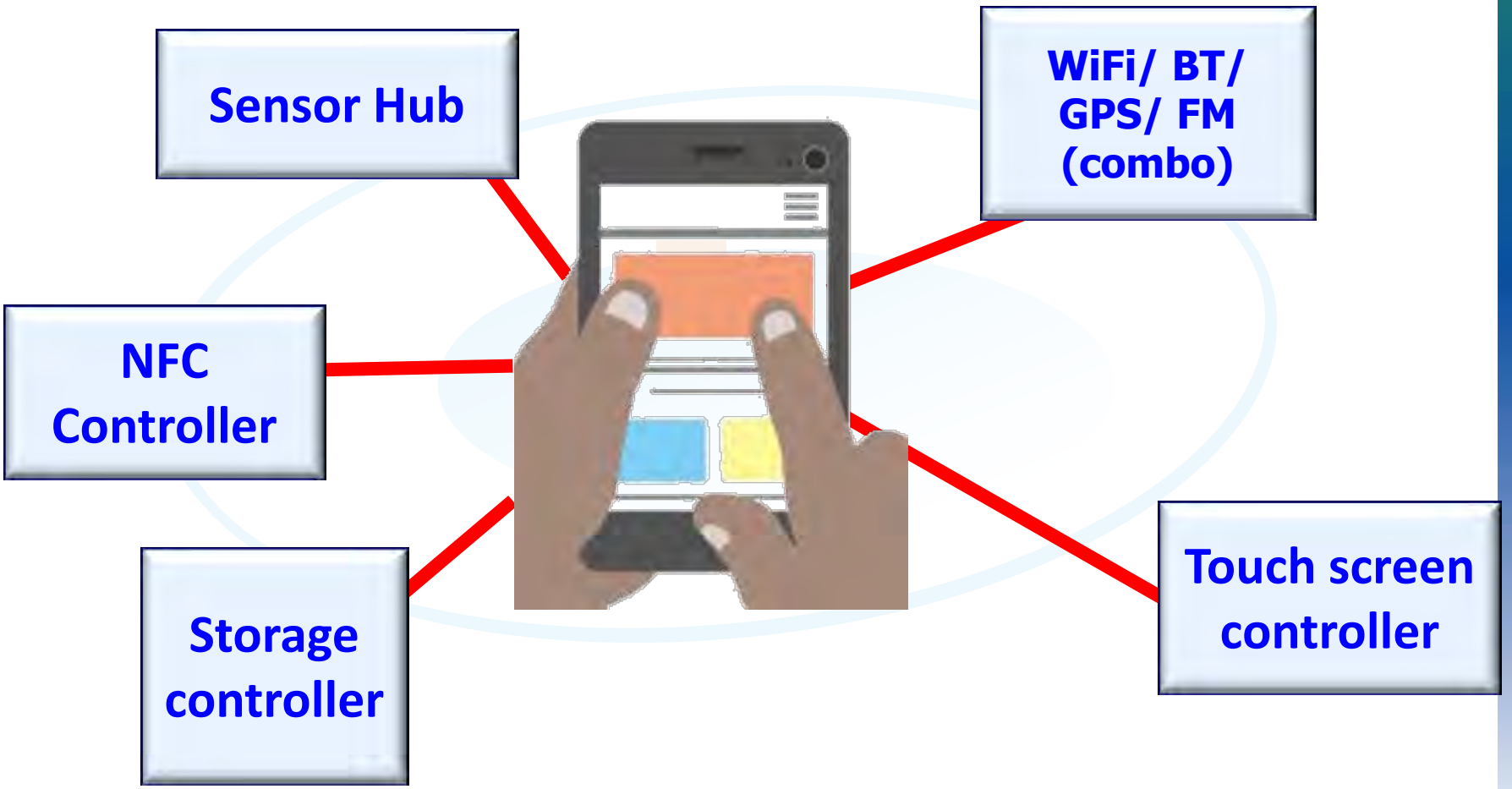
WiFi/GPS/FM/Bluetooth combo

GPS/Beido in shared bikes

Contactless payment (NFC)

晶心嵌入智能手機

1 in 5 Smart Phones are with Andes Embedded worldwide



晶心嵌入消費性裝置、車用電子及資料處理中心

Switch:
MXIC Flash Ctlr

Echo Dot2:
Mediatek WiFi IoT

Bike Sharing:
GPS Ctrl

X-Trail:
ADAS Ctlr

- In leading machine learning computers for datacenter
- In tier-one switch routers for datacenter

- Recent applications: 5G networking, 802.11ax, machine learning processors (using Andes Custom Extension, ACE)

新產品及生態系統

完整產品線

- New A-series Cores released in Andes Embedded Forum 2018

ANDES

RISC-V

晶心 RISC-V 產品概述

Best extensions to RISC-V

AndeStar™ Architecture V5

Highly optimized design with leading PPA

AndesCore™ Processors

AndeSight™ Tools

Professional IDE with high code quality

Andes Embedded™

Handy peripheral IPs to speed up SoC construction

Extensive SW stacks from bare metal, RTOS to Linux

AndeShape™ Platforms

AndeSoft™ Stacks

V5 AndesCore™ 處理器核心

N22

N25F/NX25F

A25/AX25

A25MP/AX25MP

將晶心的優勢帶進 RISC-V 處理器家族

- Architecture beyond the kernel for diversified requirements
- Efficient processor pipeline for leading PPA
- Platform IP support to help speed up SoC construction
- AndeSight IDE, and compiler/library optimizations
- RTOS and Linux support, and middleware (such as IoT stacks)
- Commercial-grade verification for all products
- Mass production experience with high quality deliverables
- Professional supporting infrastructure

最新產品路線圖

Launch of RISC-V Core IP Series

Cache-Coherent Multicores

- **A25MP**[a]: V5, 32b, 1~4 Cores; L2 Cache Coherence; DSP, MMU, FPU, ACE ...
- **AX25MP**[a]: V5, 64b, 1~4 Cores; L2 Cache Coherence; DSP, MMU, FPU, ACE ...

Linux and FPU/DSP

- **A25**: V5, 32b, 5-stage, >1.2GHz, MMU/PMP, DSP, FPU, ACE ...
- **AX25**: V5, 64b, 5-stage, >1.2GHz, MMU/PMP, DSP, FPU, ACE ...

Fast/Compact, FPU/DSP

- **D25F: +DSP**
- **N25F**: V5, 32b, 5-stage, >1.2GHz PMP, FPU, ACE...
- **NX25F**: V5, 64b, 5-stage, >1.2GHz PMP, FPU, ACE...

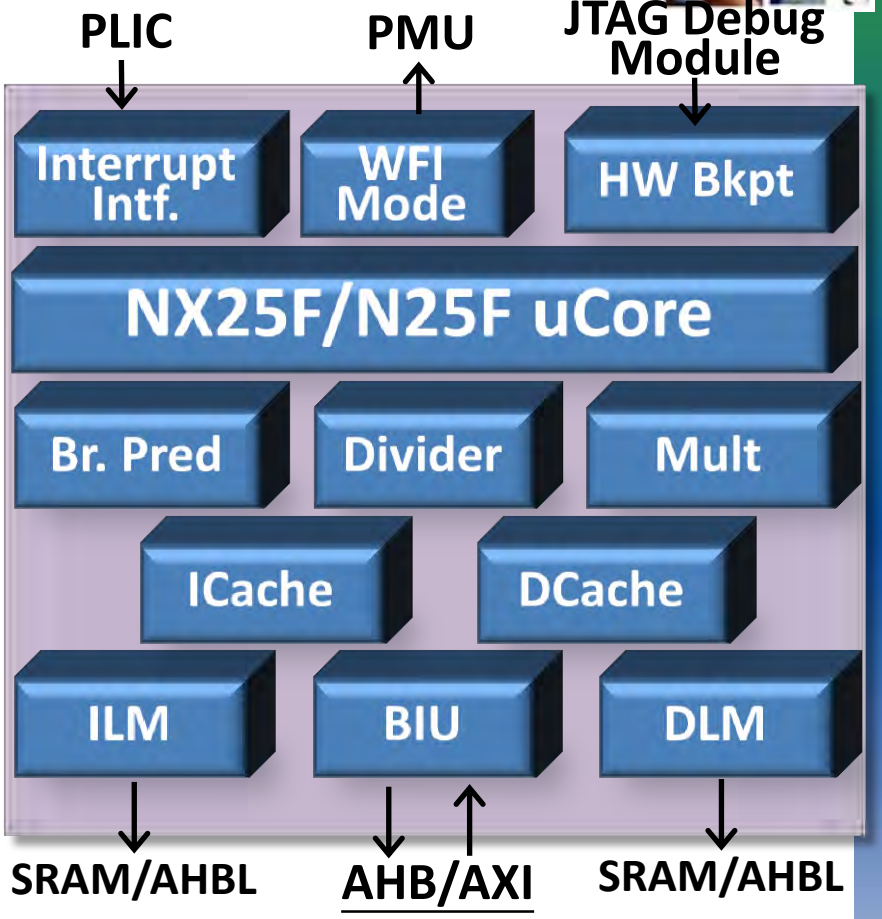
Slim and Efficient

- **N22**: V5/V5e, 32b, 2-stage 800MHz, 16/32 GPR
- ***D22F***: V5/V5e, 32b, 2-stage 800MHz, 16/32 GPR, DSP, FPU

a. A25*MP: available Q1/2019
b. 28HPC+ RVT, SS, 0.81V, 0C, with I/O constraints.

V5 AndesCores: 25-系列

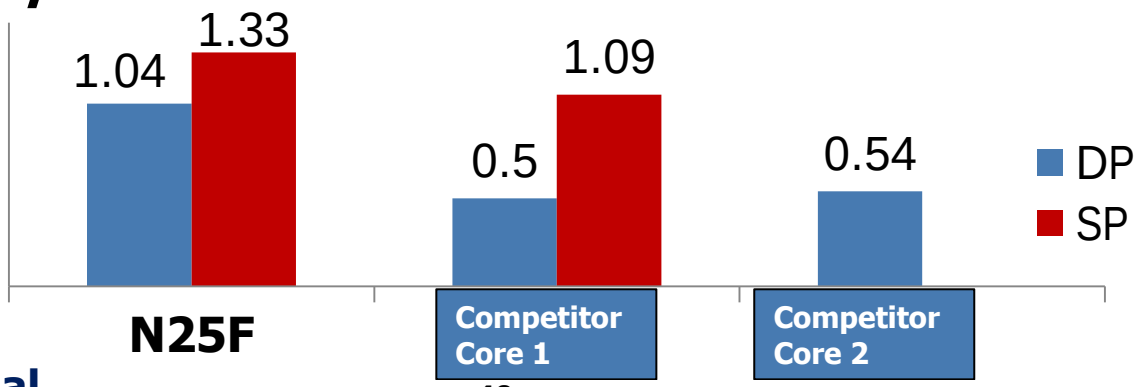
- **N25F: 32-bit, NX25F: 64-bit**
  - From scratch for the best PPA
  - Very configurable
- **AndeStar V5 ISA**
- **5-stage pipeline**
- **Configurable multiplier**
- **Optional branch prediction**
- **Flexible memory subsystem**
  - I/D Local Memory (LM): to 16MB
  - I/D caches: up to 64KB, 4-way
  - Optional parity or ECC
  - Hit-under-miss caches
  - load/store: unaligned accesses



- **N25F sample configurations @TSMC 28HPC+ RVT:**
  - Small config: 37K gates, 1.0 GHz (worst case)
  - Large config: 130K gates, 1.2GHz (worst case)
  - **Best-in-class Coremark: 3.58/MHz**

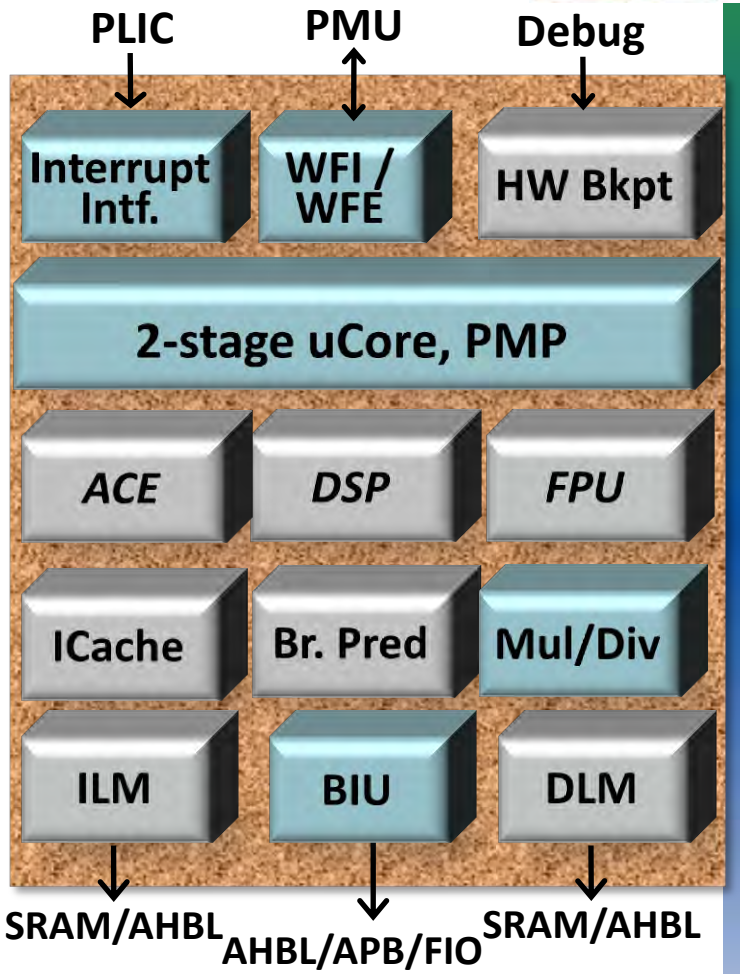
V5 AndesCores: 25-系列

- **Fast-n-small for control tasks in AR/VR, networking, storage, AI**
- **N25F/NX25F: +FPU**
  - +, −, x, x+, x−: pipelined 4 cycles
  - ÷, √ : run in the background
    - ◆15 for SP, 29 for DP
  - FP load/store: support HP
- **A25/AX25: +FP +Linux**
  - Support RISC-V MMU and S-mode
  - 4 or 8-entry ITLB and DTLB
  - 4-way 32~128-entry Shared-TLB
- **Whetstone/MHz**:



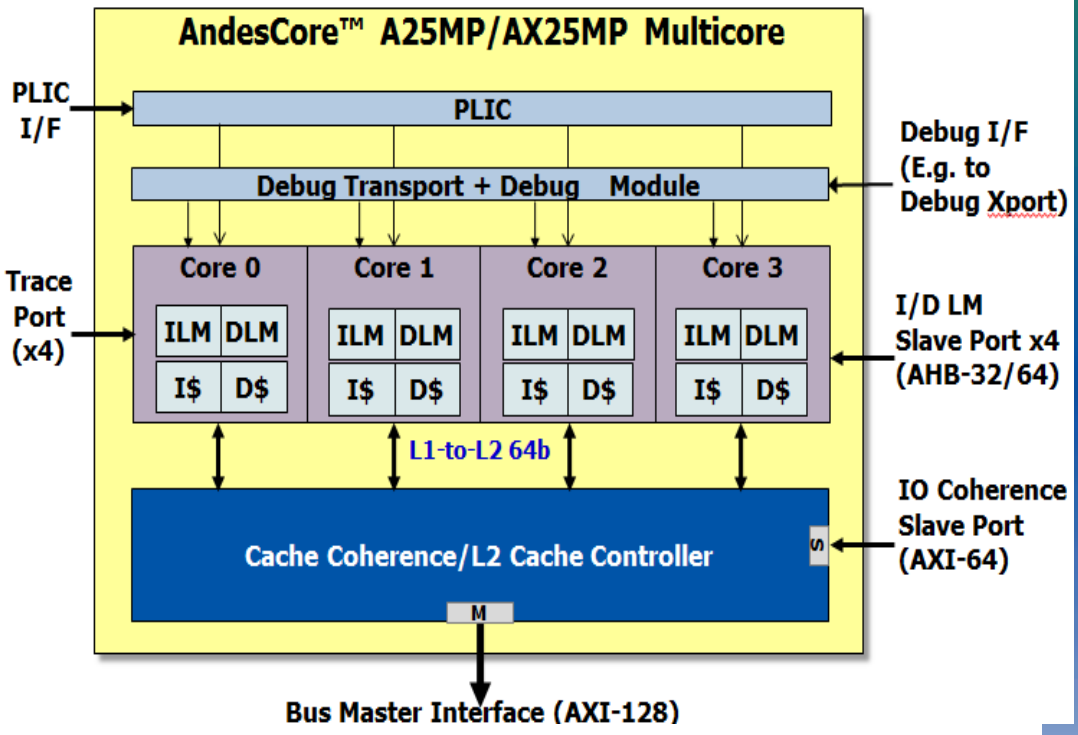
V5 AndesCores: 22-系列

- **AndeStar V5 or V5e ISA**
  - RV32-IMC or RV32-EMC
  - Plus Andes extension
- **2-stage pipeline with AHB-lite main bus**
- **Rich baseline options:**
  - I/D Local Memory (1KB~512MB), I cache
  - Fast or small multiplier, branch predictions
  - Up to 16-entry PMP, StackSafe
  - M-mode, or M+U-mode
  - APB private peripheral port, fast IO port
  - WFI, WFE, and PowerBrake
  - Vectored and preemptive interrupt controller
- **Advanced options: *ACE, DSP, FPU***
- **28nm PPA:**
  - **>750 MHz** (worst case)
  - **<15K gates** (minimal)
- **Best per-MHz performance:**
  - **1.8 DMIPS** (no inline)
  - **3.97 Coremark**



A(X)25MP Cache-Coherent Multicore

- **1/2/4 A25 (32-bit)/AX25 (64-bit) CPUs**
  - RV-IMACFD ISA, supporting SMP Linux
  - With the latest P-extension (DSP/SIMD ISA), Andes' contribution to RISC-V
- **Hardware Multicore Cache Coherence**
  - Support MESI cache coherence protocol by ACU (Andes Coherence Unit)
  - Support I/O coherence without data caches
- **Level-2 Cache Controller**
  - 0/128/256K...2MB, 32-byte line, 16-way
  - ECC, SECDED support
- **Bus Interfaces**
  - AXI bus master interface
  - Local memory slave port, for each A25/AX25 CPU
  - I/O coherence slave port
  - MP subsystem vs. bus interface synchronous N:1 clock ratio
- **Platform Level Interrupt, Debug and Trace Support**



ACE: Andes Custom Extension

Verilog user.v

concise RTL

semantics, operands, test-case spec

script user.ace

COPILOT

Custom-OPtimized Instruction deveLOpment Tools

Automated Env. For Cross Checking

Test Case Generator

Extended RTL

Extended ISS

Extended Tools + Compiler Asm/Disasm Debugger IDE

Extended ISS + CPU ISS (near-cycle accurate)

Extended RTL + CPU RTL

Extensible Baseline Components

Executable or library

Source file

積極參與RISC-V社群活動

Foundation Task Groups (partial list)

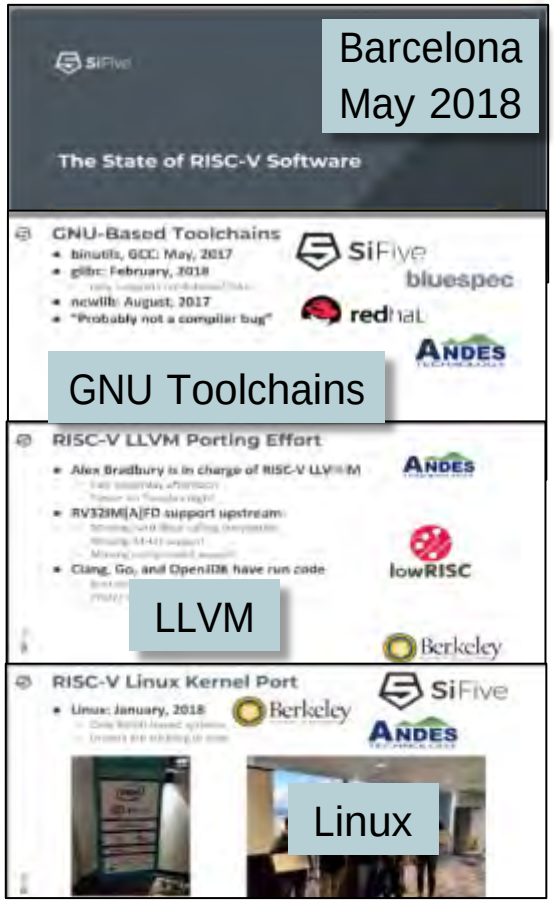
- **Contributing hardware architecture extensions**
  - **Chair of the P-extension (Packed SIMD/DSP) Task Group**
  - **Co-chair of Fast Interrupts Task Group**
  - **Closely reviewing activities of other Task Groups**

晶心協助強化RISC-V生態系統

- More choices for customers are good
- Andes works closely with partners to grow RISC-V ecosystem

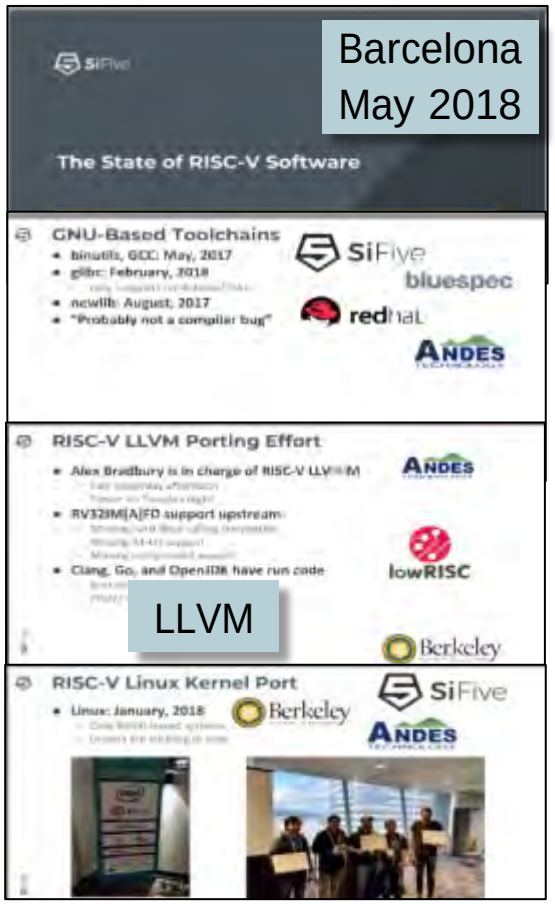
RISC-V 軟體生態系統: GNU Toolchain

- **GCC, binutils**: May, 2017
- **Newlib**: Aug, 2017
- **Glibc (rv64i)**: Feb, 2018
- **GDB**: Mar, 2018
- **OpenOCD**: July, 2018
- **Glibc (rv32i)**:
  - Submitted in July 2018 (by Andes)
  - Review in progress



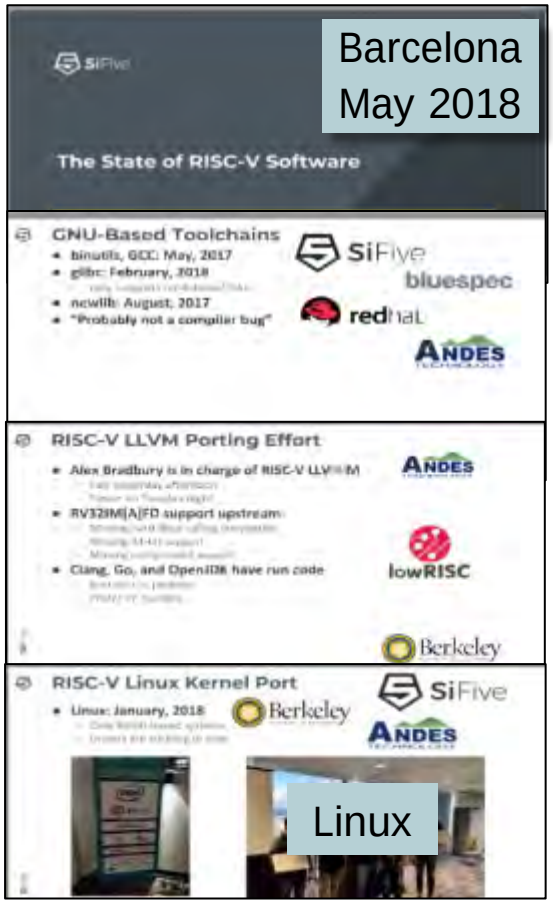
RISC-V 軟體生態系統: LLVM Compilation

- **LLVM**:
  - RV32IMAFDC: June, 2018
  - Relaxation: May, 2018 (by Andes)
  - 64b support: Nov, 2018
  - Missing hard-float calling convention
- **compiler-rt**: Mar, 2018
- **LLD**: Aug, 2018 (by Andes)
  - Initial port (relocation and TLS) in Oct. 2017
  - Dynamic linking review in progress since Oct, 2017
  - Missing link-time relaxation



RISC-V 軟體生態系統: Linux

- **U-boot**: Jan, 2018 (by Andes)
- **Kernel (rv64i)**: Jan, 2018
- **Key utilities**: (by Andes)
  - Perf: Feb, 2018
  - Kernel Module: May, 2018
  - Ftrace: May, 2018
- **Kernel (rv32i)**: Jun, 2018 (by Andes)
- **Kernel with CONFIG_FPU**: Oct, 2018 (by Andes)



晶心在 RISC-V 上的定位

完整的產品組合

可靠的 **RISC-V** 核心 **IP** 供應商

可在**Linux**環境中執行的**RISC-V** 處理器核心

超低功耗、高運算效能的處理器核心

領先世界推出具有客戶可自訂指令的**RISC-V**處理器核心

2018年 RISC-V 客戶分析

- **Sixteen design wins for Andes RISC-V Core IPS:**
  - **NX25: Enterprise SSD (Taiwan)**
  - **N25: AI (China w/ ACE), Blockchain (China), HD-PLC (Japan), SSD (China), Fingerprint (Taiwan), AI (China x2), TDDI (Taiwan), SD/eMMC (Taiwan), Research/Academic (Taiwan x2)**
  - **N25/AX25: FPGA for AI (US)**
  - **AX25: FPGA for AI (China)**
  - **A25: 5G (US), Automotive (Korea)**
- **Thirteen design service providers joined Andes RISC-V Easy Start Program:**
  - **US x 3, Europe x1, Korea x 1, China x 3, Taiwan x 5**

AndesCore™ 競爭優勢

AndesCore™	AndesCore/ Competitor Power Efficiency[1] (DMIPS/mW)	Competitors
N7	+42%	Cortex-M0+
N8	+43%	Cortex-M3
N9	+43%	Cortex-M3
D10	+48%	Cortex-M4
N13	+185%	Cortex-A5
N13	+45%	Cortex-R4
D15F	+121%	Cortex-M7

1. Power Efficiency is DMIPS/MHz divided by power consumption (mW/MHz) when running Dhrystone.

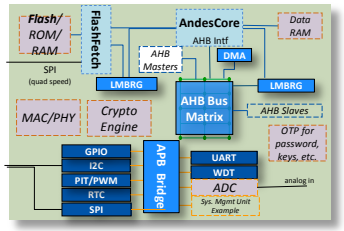
生態系統: Andes 與 Knect.me

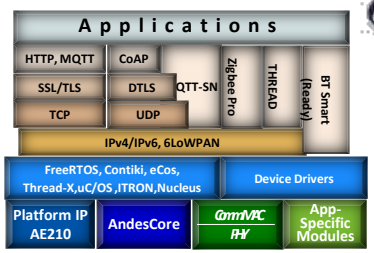
ANDES TECHNOLOGY

knectme™

Knect.me 生態系統

- **Built up Ecosystem *knect.me* to help IoT Developing**
  - to **knect** solutions - Silicon IP's, SW stacks, tools, applications, systems and products
- **Includes:**
  - SoC IP Platforms
  - Software Stack
  - Development Boards
  - Development Tools
- **To Form a IoT League**
  - to **knect** chip vendors, partners, application developers, system vendors





近期獲獎

ANDES TECHNOLOGY

引領新興科技潮流

- **"2018 Top25最佳新興科技解決方案提供公司"**

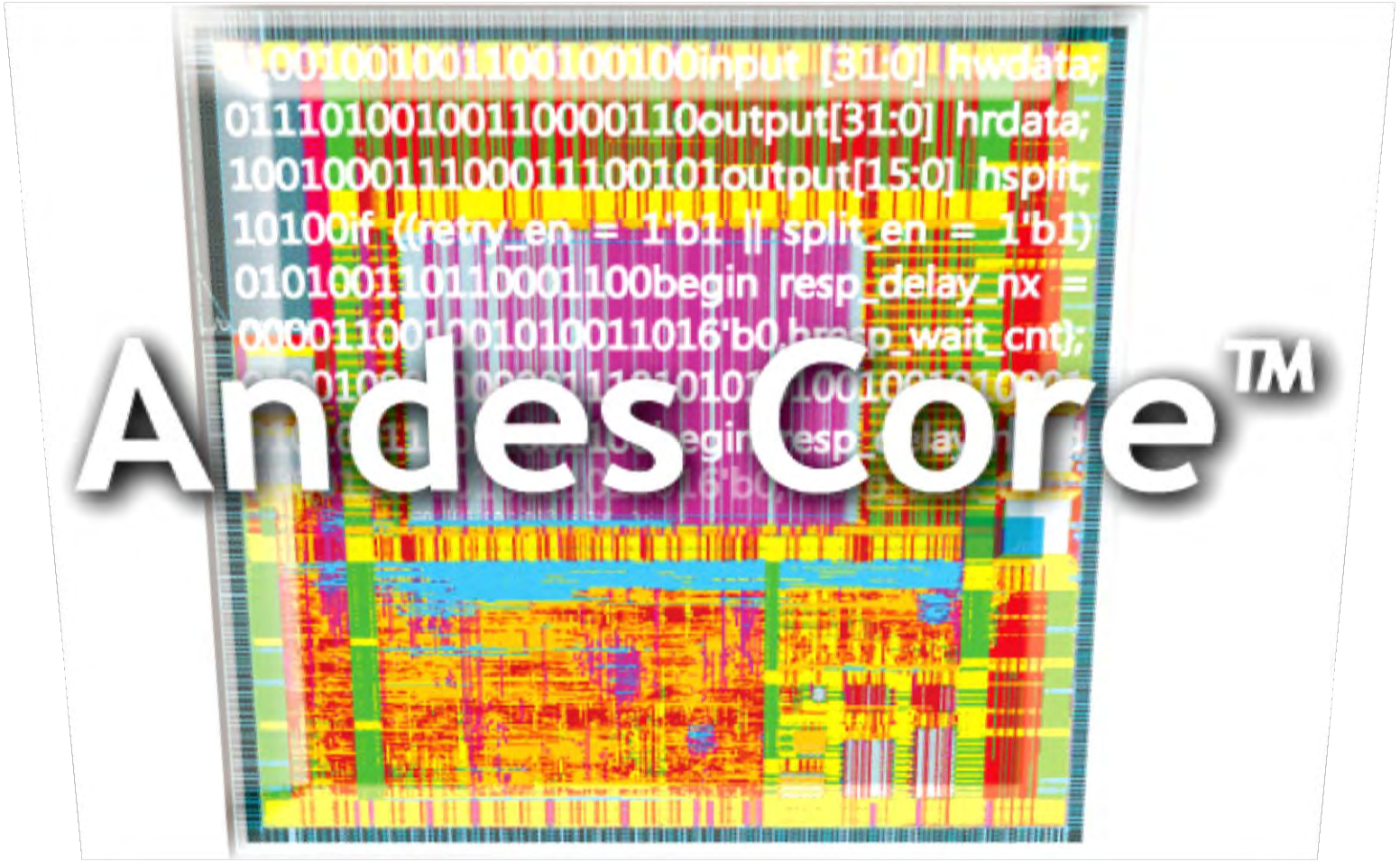
— CIO Advisor Magazine

總結

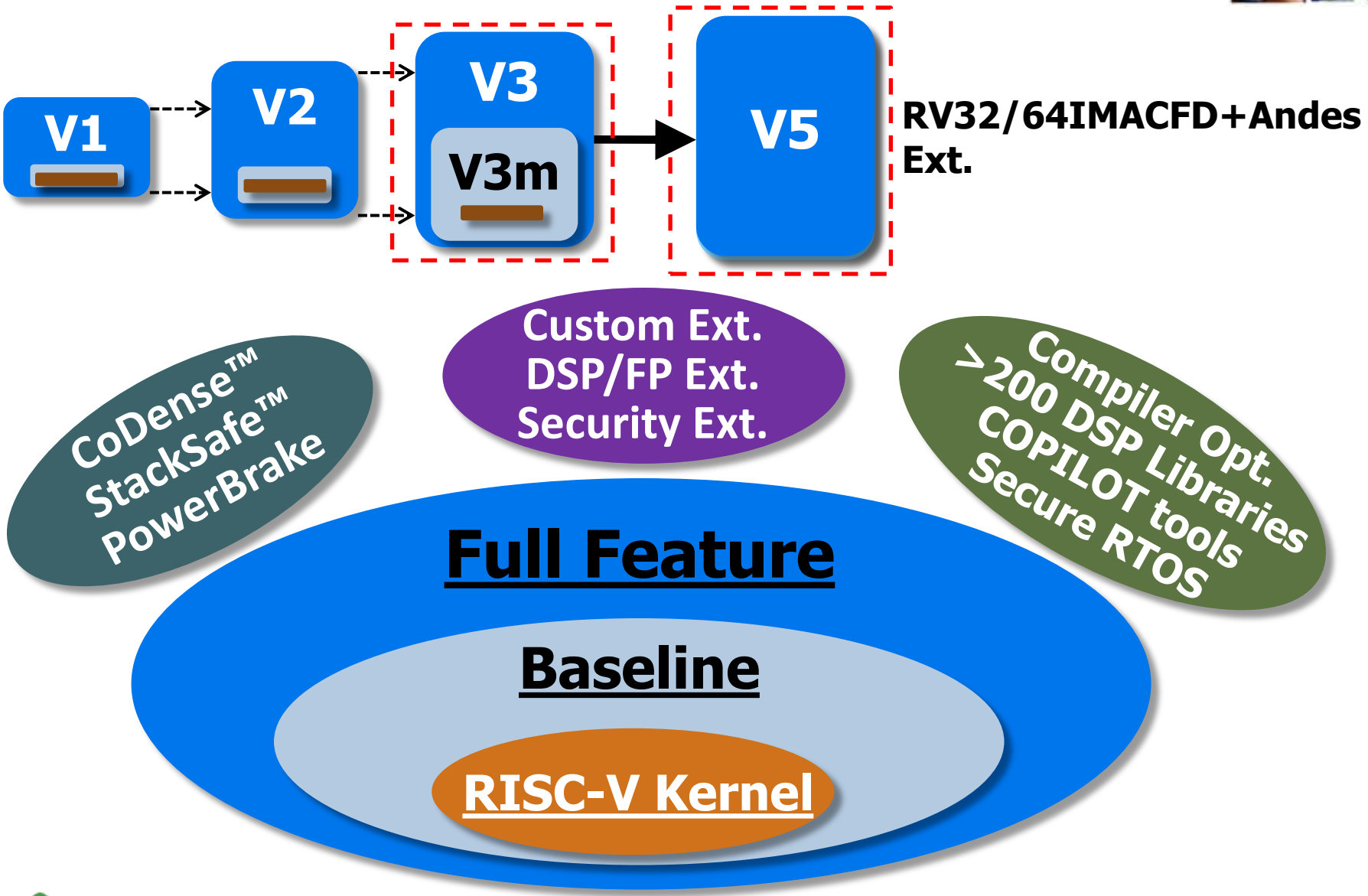
晶心科技擴大產品陣線,強化生態系統

- 晶心科技發布了新的RISC-V處理器核心 (N22, A(X)25MP, D25F)，適合更多的客戶應用。
- 晶心科技積極參與 RISC-V 基金會科技與社群發展，並與RISC-V 生態系統互助。
- 晶心科技持續與全球 Design service houses簽訂合約，授權其協助客戶開發內嵌 Andes RISC-V core的ASIC (稱為Andes RISC-V Easy Start Program)，創造晶心、Design service house與產業共贏的局面。

謝謝指教



www.andestech.com

問與答

AndeStar™ V5:新一代的 ISA Kernel