Safe Harbor Notice

Except for the historical information contained herein, the matters addressed in this presentation are forward-looking statements that involve certain risks and uncertainties that could cause actual results to differ materially, including but not limited to weather, impact of competitive products and pricing, industry-wide shifts in the supply and demand for semiconductor products, rapid technology change, semiconductor industry cycle, and general economic conditions.

Except as required by law, Andes undertake no obligation to update any forward-looking statement, whether as a result of new information, future events or otherwise.
Agenda

- Overview of Andes Technology Corporation
- Operating Results
- Product Application
- New Products and Ecosystems
- Andes Awarded
- Concluding Remarks
Overview of Andes Technology Corporation

Andes Highlights

- Founded in March 2005 in Hsinchu Science Park, Taiwan, ROC.
- Core RD team from AMD, DEC, Intel, MIPS, nVidia, and Sun veterans.
- Under 150 people now; 80% are engineers.
- EETimes' Silicon 60 Hot Startups to Watch (2012)
- TSMC OIP Award “Partner of the Year” for New IP (2015)
- A founding member of RISC-V Foundation (2016)
- IPO in Taiwan Stock Exchange (March 2017)

Andes Mission

- Innovate performance-efficient processor solution for low-power SoC

Emerging Opportunities

- Smart and Green electronic devices
- Cloud Computing, Artificial Intelligence and Internet of Things
Operating Results
Agreement Growth Analysis

<table>
<thead>
<tr>
<th>Year</th>
<th>IP agreements</th>
<th>Accumulated IP agreements</th>
</tr>
</thead>
<tbody>
<tr>
<td>2006</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>2007</td>
<td>2</td>
<td>3</td>
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<tr>
<td>2008</td>
<td>3</td>
<td>6</td>
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<tr>
<td>2009</td>
<td>6</td>
<td>12</td>
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<tr>
<td>2010</td>
<td>12</td>
<td>16</td>
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<tr>
<td>2011</td>
<td>16</td>
<td>24</td>
</tr>
<tr>
<td>2012</td>
<td>24</td>
<td>40</td>
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<tr>
<td>2013</td>
<td>27</td>
<td>56</td>
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<tr>
<td>2014</td>
<td>27</td>
<td>80</td>
</tr>
<tr>
<td>2015</td>
<td>31</td>
<td>107</td>
</tr>
<tr>
<td>2016</td>
<td>39</td>
<td>134</td>
</tr>
<tr>
<td>2017</td>
<td>21</td>
<td>165</td>
</tr>
<tr>
<td>2018</td>
<td>225</td>
<td></td>
</tr>
</tbody>
</table>
Consolidated Revenue

- **2Q18 Revenue**: NT$88.08M
- **YoY**: Up 5.3%
- **QoQ**: Up 154%

(NT$ thousands)

<table>
<thead>
<tr>
<th>Quarter</th>
<th>Revenue</th>
</tr>
</thead>
<tbody>
<tr>
<td>2Q17</td>
<td>83,628</td>
</tr>
<tr>
<td>1Q18</td>
<td>34,681</td>
</tr>
<tr>
<td>2Q18</td>
<td>88,087</td>
</tr>
</tbody>
</table>
Royalty Analysis

YoY 42.3%
QoQ 47.9%

(NT$ thousands)

<table>
<thead>
<tr>
<th></th>
<th>2Q17</th>
<th>1Q18</th>
<th>2Q18</th>
</tr>
</thead>
<tbody>
<tr>
<td>Royalty</td>
<td>9,876</td>
<td>9,501</td>
<td>14,053</td>
</tr>
</tbody>
</table>
Royalty Analysis

(NT$ thousands)

: 2018 H1 royalty collected

<table>
<thead>
<tr>
<th>Year</th>
<th>Royalty</th>
<th>Customer numbers</th>
</tr>
</thead>
<tbody>
<tr>
<td>2011</td>
<td>445</td>
<td>1</td>
</tr>
<tr>
<td>2012</td>
<td>660</td>
<td>2</td>
</tr>
<tr>
<td>2013</td>
<td>1,285</td>
<td>5</td>
</tr>
<tr>
<td>2014</td>
<td>10,819</td>
<td>9</td>
</tr>
<tr>
<td>2015</td>
<td>12,232</td>
<td>15</td>
</tr>
<tr>
<td>2016</td>
<td>13,320</td>
<td>15</td>
</tr>
<tr>
<td>2017</td>
<td>38,287</td>
<td>25</td>
</tr>
<tr>
<td>2018</td>
<td>$23,554</td>
<td></td>
</tr>
</tbody>
</table>

2018 H1 royalty collected (NT$ thousands)
Consolidated Gross Margin

(NT$ thousands)

<table>
<thead>
<tr>
<th></th>
<th>2Q17</th>
<th>1Q18</th>
<th>2Q18</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gross Profit</td>
<td>83,341</td>
<td>34,548</td>
<td>88,001</td>
</tr>
<tr>
<td>Gross Margin</td>
<td>99.7%</td>
<td>99.6%</td>
<td>99.9%</td>
</tr>
</tbody>
</table>
Consolidated Operating Expenses

(NT$ thousands)

YoY
-22%

QoQ
+14.8%

<table>
<thead>
<tr>
<th></th>
<th>2Q17</th>
<th>1Q18</th>
<th>2Q18</th>
</tr>
</thead>
<tbody>
<tr>
<td>Selling expenses</td>
<td>29,465</td>
<td>19,123</td>
<td>21,129</td>
</tr>
<tr>
<td>Administration expenses</td>
<td>13,821</td>
<td>12,644</td>
<td>17,567</td>
</tr>
<tr>
<td>R&amp;D expenses</td>
<td>38,693</td>
<td>23,933</td>
<td>25,270</td>
</tr>
</tbody>
</table>

Legend:
- Selling expenses
- Administration expenses
- R&D expenses
Consolidated Operating Margin

YoY
+25.7pt

QoQ
+88.3pt

2Q17
1Q18
2Q18

1.6%

27.3%

-61.0%
Consolidated Net Profit (Loss) Margin

YoY
+29.9pt

QoQ
+95.2pt

3.7%

33.6%

-61.6%

2Q17
1Q18
2Q18
Consolidated Earnings Per Share

<table>
<thead>
<tr>
<th>Quarter</th>
<th>QoQ</th>
<th>YoY</th>
</tr>
</thead>
<tbody>
<tr>
<td>Q2 2017</td>
<td>-0.20</td>
<td>0.08</td>
</tr>
<tr>
<td>Q1 2018</td>
<td>0.40</td>
<td>0.73</td>
</tr>
<tr>
<td>Q2 2018</td>
<td>0.60</td>
<td>(0.53)</td>
</tr>
</tbody>
</table>

(NT$ dollars)

YoY: +0.65
QoQ: +1.26
1H18 Revenue Analysis by Payment Model

- **License**: 74%
- **Royalty**: 19%
- **Maintenance and others**: 7%
1H18 Revenue Analysis by Region

- Taiwan: 44%
- China: 37%
- USA: 9%
- Europe: 6%
- Japan/Korea: 4%

Driving Innovations™
1H18 Revenue Analysis by Product

- N10: 27%
- N9: 17%
- N25: 15%
- N8: 9%
- N13: 8%
- D10: 5%
- D15: 4%
- D13: 4%
- N25: 3%
- N7: 1%
- Platform IP: 1%
- AX25: 1%
- A25: 1%
- N6: 4%
- NX25: 4%
- N10: 8%

17
1H18 Customer Application Analysis

- Artificial Intelligence: 14%
- Audio: 5%
- IoT: 38%
- MCU: 10%
- Navigation: 9%
- Storage: 5%
- Networking: 5%
- Video: 14%

*Based on agreements number*
## 1H18 Design Win

- Agreements may sign for H1: 20 ~ 23 reported, now 21

<table>
<thead>
<tr>
<th></th>
<th>Jan - June</th>
<th>Subtotal</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>N7, N8, N9</strong></td>
<td>Mainland x 4, US x 2, Korea x 3, Taiwan x 1</td>
<td>10</td>
</tr>
<tr>
<td><strong>N10, D10, N13</strong></td>
<td>Mainland x 4, US x 1, Taiwan x 1</td>
<td>6</td>
</tr>
<tr>
<td><strong>D15</strong></td>
<td>Europe x 1</td>
<td>1</td>
</tr>
<tr>
<td><strong>N25, NX25, AX25</strong></td>
<td>Mainland x 2, US x 1, Taiwan x 1</td>
<td>4</td>
</tr>
</tbody>
</table>
RI SC-V Revenue Share Ramping

(NT$ thousands)

<table>
<thead>
<tr>
<th>Quarter</th>
<th>RISC-V</th>
<th>V3</th>
</tr>
</thead>
<tbody>
<tr>
<td>1Q18</td>
<td>4,376</td>
<td>30,305</td>
</tr>
<tr>
<td>2Q18</td>
<td>27.1%</td>
<td>64,230</td>
</tr>
</tbody>
</table>

12.6%
Product Application
Rich Customers’ Applications

- Touch Screen
- eBook/eDictionary
- Power management
- Bio-medical device
- CMMB
- MCU
- TCON
- Wireless display
- WiFi, Bluetooth
- GPS, GPON, NFC
- Gateway/router
- Portable Karaoke
- Sigfox LPWAN
- IoT Cat0 base station
- IoT MCU
- ESL
- Smart Meter
- Smart Lighting
- USB3.0
- SSD, eMMC
- Anti-virus
- Sensor Hub
- mSATA
- Secure SD
- Fingerprint Recognition
- Motor Control
- Wireless Charger
- Surveillance
- Barcode scanner
- ADAS
- VEDR
- 4K2K CODEC
- 8K4K CODEC
- and more.....
IoT Application - 1

- Bluetooth Speaker
- Sigfox LPWAN
- Healthcare device
- Wearable device
- Electronic price tags
- Sensor Hub
IoT Application - 2

- Wearable devices
- GPS/Beido in shared bikes
- Portable Karaoke
- WiFi/GPS/FM/Bluetooth combo
- Contactless payment (NFC)
- Drone
Automotive Applications

- **N13**
  - Calibration of AVM (Around View Monitoring) in NISSAN New X-Trial

- **N10**
  - CAR Event Recorder
  - ADAS

- **D10**
  - ADAS
AI Applications

- **N9** Dataflow Processing
- **D10** Voice Recognition

Courtesy: Wave Computing

**Andes Embedded™**

- **D15F** Video recognition
- **N9** AI companion

Andes Core

SoC for WiFi in AI Companion

Yes, boss, I understand...
Emerging Applications

❖ AI
  ▪ Deep Learning
❖ Next generation TV
❖ Network Engine
  ▪ Router
❖ Drone
❖ Robot
❖ …
❖ Many new applications are emerging
New Products and Ecosystems
Product Lines

New Core released in Andes Embedded Forum 2018

ANDES

RISC-V
V5 AndesCore™ Processors

N25/NX25
N25F/NX25F
A25/AX25
AndeStar™ V5: New Generation of ISA Kernel

V1 → V2 → V3m → V5

- CoDense™
- StackSafe™
- PowerBrake

- Full Feature
- Baseline
- RISC-V Kernel

- Custom Ext.
- DSP/FP Ext.
- Security Ext.

- Compiler Opt.
- >200 DSP Libraries
- COPILLOT tools
- Secure RTOS

V5m+ more Andes Ext.
RV32/64I MAC+ Andes Ext.
AndesCore™ V5 families

**Ultra Performance**
- A25*
  - V5m, 32-bit 5-stage, 1GHz
  - MMU/MPU, PMP, FPU, ACE...
- AX25*
  - V5m, 64-bit 5-stage, 1GHz
  - MMU/MPU, PMP, FPU, ACE...

**Enhanced Features**
- N25F*
  - V5m, 32-bit 5-stage, 1GHz
  - PMP, FPU, ACE...
- NX25F*
  - V5m, 64-bit 5-stage, 1GHz
  - PMP, FPU, ACE...

**Modern Architecture**
- N25
  - V5m, 32-bit 5-stage, 1GHz
  - Compact
- NX25
  - V5m, 64-bit, 5-stage, 1GHz
  - Compact

- 28HPC RVT, SS, 0.81V, 0C, with I/O constraints. * Available now

Andes Confidential
Driving Innovations™
Baseline V5 AndesCore™: N25/ NX25

- Fast-n-small cores for control tasks in storage, networking, AI, and more.
- N25: 32-bit, NX25: 64-bit
  - From scratch for the best PPA
- AndeStar V5m ISA
  - Superset of RV-IMAC
- 5-stage pipeline
- Configurable multiplier
  - Sequential or parallel
- Optional branch prediction
- Flexible memory subsystem
  - I/D Local Memory (LM): to 16MB
  - I/D caches: to 64KB
  - Optional parity or ECC
- Bus interface
- JTAG debug module

- N25 sample config. @ 28HPC:
  - Small: 37K gates, 1GHz (worst)
  - Large: 159K gates, 1.15GHz (worst)
New V5 AndesCores Coming this Summer

- **4 New 25-series**: maintain the frequency
  - **N25F/NX25F**: N25/NX25 + FP support
  - **A25/AX25**: N25F/NX25F + MMU + S-mode

- **High-performance FP support**:
  - IEEE754-compliant single/double precisions
  - Multiply, add/sub, multiply-accumulate:
    - 1-cycle issue rate, 4-cycle latency
  - Divide/sqrt: 15 cycles for SP, 29 cycles for DP
    - Run in the background
  - **Half-precision** load/store for machine learning

- **MMU support**:
  - Supporting SV{32, 39, 48}
  - Page size: {Kilo, Mega, Giga, Tera} page
  - 4- or 8-entry microTLBs (ITLB, DTLB)
  - 4-way 32~128-entry Shared-TLB (STLB)
Andes Position in RISC-V

- Complete product portfolio
- Reliable RISC-V core IP business partner
- RISC-V core that runs Linux
- Extreme low power consumption, high computing efficiency
- World’s only Customer-Extension Capable RISC-V Core
YTD RISC-V Design Win

- NX25: Enterprise SSD (Taiwan)
- N25, AX25: FPGA for AI (US)
- N25: AI (China)
- AX25: FPGA for AI (China)
- Six design service providers joined Andes RISC-V Easy Start Program: US x 2, Korea x 1, China x 1, Taiwan x 2
## Summary of AndesCores vs. Competitors

<table>
<thead>
<tr>
<th>AndesCore™</th>
<th>AndesCore/Competitor Power Efficiency¹ (DMIPS/ mW)</th>
<th>Competitors</th>
</tr>
</thead>
<tbody>
<tr>
<td>N7</td>
<td>+42%</td>
<td>Cortex-M0+</td>
</tr>
<tr>
<td>N8</td>
<td>+43%</td>
<td>Cortex-M3</td>
</tr>
<tr>
<td>N9</td>
<td>+43%</td>
<td>Cortex-M3</td>
</tr>
<tr>
<td>D10</td>
<td>+48%</td>
<td>Cortex-M4</td>
</tr>
<tr>
<td>N13</td>
<td>+185%</td>
<td>Cortex-A5</td>
</tr>
<tr>
<td>N13</td>
<td>+45%</td>
<td>Cortex-R4</td>
</tr>
<tr>
<td>D15F</td>
<td>+121%</td>
<td>Cortex-M7</td>
</tr>
</tbody>
</table>

¹ Power Efficiency is DMIPS/ MHz divided by power consumption (mW/ MHz) when running Dhrystone.
64 Bit Infrastructure and Eco-System

**Processor Architecture**

**AndeStar™**

V5, V5m

**Processor IP’s**

**AndesCore™**

NX25

**Development Platforms**

**AndeShape™**

**Development Tools**

**AndeSight™**

**SW Stacks**

**AndeSoft™**
Two Ecosystems: Andes and Knect.me
Knect.me Ecosystem

- Built up Ecosystem **knect.me** to help IoT Developing
  - to **knect** solutions - Silicon IP’s, SW stacks, tools, applications, systems and products
- Includes:
  - SoC IP Platforms
  - Software Stack
  - Development Boards
  - Development Tools
- To Form a IoT League
  - to **knect** chip vendors, partners, application developers, system vendors
Added A.I. to Knect.me Ecosystem

What is “IoT League”? We invite Andes’ customers to provide products information which contains AndesCore. IoT League can enhance exposure and reputation in IoT domain. Various applications can help Andes’ customers to attract more and more users to adopt their IoT products.

Companies in alphabetical order
Andes Awarded
Leader of the Emerging Technology

“2018 Top25 emerging tech solutions provider”
— CIO Advisor Magazine
Concluding Remarks
Andes: Even Better Value in Future

- Andes aggressively involved in RISC-V Foundation new technology and clusters development, contributing and leveraging RISC-V eco-system. For example, GCC compiler, LLVM compiler, fast interrupt, vector instructions, etc. Andes now leads RISC-V DSP instruction set working group in developing RISC-V P-extension specification discussion and future releasing.

- Andes has successively signed six contracts with design service houses to authorize ASIC design to embed RISC-V core (Andes RISC-V Easy Start Program). Such alliance program will continue, Andes targets to sign up 20 design service houses worldwide in a few months. These contracts will create a win-win situation for Andes, the design service houses and the end customers.
Thank You!

www.andestech.com
Q&A