Safe Harbor Notice

Except for the historical information contained herein, the matters addressed in this presentation are forward-looking statements that involve certain risks and uncertainties that could cause actual results to differ materially, including but not limited to weather, impact of competitive products and pricing, industry-wide shifts in the supply and demand for semiconductor products, rapid technology change, semiconductor industry cycle, and general economic conditions.

Except as required by law, Andes undertake no obligation to update any forward-looking statement, whether as a result of new information, future events or otherwise.
Agenda

- Overview of Andes Technology Corporation
- Operating Results
- Product Applications
- New Products and Ecosystems
- Andes Awarded
- Concluding Remarks
Overview of Andes Technology Corporation

**Andes Highlights**

- Founded in March 2005 in Hsinchu Science Park, Taiwan, ROC.
- Core RD team from AMD, DEC, Intel, MIPS, nVidia, and Sun veterans.
- Over 160 people now; 80% are engineers.
- EETimes' Silicon 60 Hot Startups to Watch (2012)
- TSMC OIP Award “Partner of the Year” for New IP (2015)
- A founding member of RISC-V Foundation (2016)
- IPO in Taiwan Stock Exchange (March 2017)

**Andes Mission**

- Innovate performance-efficient processor solution for low-power SoC

**Emerging Opportunities**

- Smart and Green electronic devices
- Cloud Computing, Artificial Intelligence and Internet of Things
Operating Results
Business Status Overview

- **>160 commercial licensees**
  - Geographically distributed in Taiwan, China, Korea, Japan, Europe, and USA.
  - **>246 license agreements signed**

- **AndeSight™ IDE:**
  - **>14,000 installations**

- **Eco-system:**
  - **>130 partners**

- **>3.6B Accumulative SoC Shipped by the end of 2018**
Agreement Growth Analysis

Year | IP agreements | Accumulated IP agreements
--- | --- | ---
2006 | 1 | 1
2007 | 2 | 3
2008 | 3 | 6
2009 | 6 | 12
2010 | 12 | 24
2011 | 16 | 40
2012 | 16 | 56
2013 | 24 | 80
2014 | 27 | 107
2015 | 27 | 134
2016 | 31 | 165
2017 | 39 | 204
2018 | 42 | 246
2018 Revenue Analysis

### YoY Growth
- **Q4 2017**: 57,034
- **Q3 2018**: 56,364
- **Q4 2018**: 125,624

YoY Growth:
- 120.3%

### QoQ Growth
- **Q4 2018** vs. **Q3 2018**:
  - YoY: +122.9%
  - QoQ: +5.3%

### Revenue Analysis
- **2017**: 289,377
- **2018**: 304,756
2018 Top 10 Customers Analysis by Revenue

Top 10 Customer Contributed 56% Revenue

(NT$ thousands)

Wireless/IoT (TW)
Touch Panel (TW)
Gaming (TW)
Storage (TW)
Wireless/IoT (TW)
Artificial Intelligence (CN)
Sensing (TW)
Automotive (KO)
Artificial Intelligence (US)
Networking (US)
Total Customers Annual and Accumulated Shipment

(Unit: M ps)

<table>
<thead>
<tr>
<th></th>
<th>2017</th>
<th>2018</th>
</tr>
</thead>
<tbody>
<tr>
<td>Annual Shipment</td>
<td>590</td>
<td>1,132</td>
</tr>
<tr>
<td>Accumulated Shipment</td>
<td>2,500</td>
<td>3,632</td>
</tr>
</tbody>
</table>
2018 Royalty Analysis

YoY +143.5%  QoQ +26.9%  YoY +95.8%

(NT$ thousands)

4Q17  3Q18  4Q18
11,805  22,655  28,744

2017  2018
38,287  74,953

+26.9%  +143.5%  +95.8%
Royalty & Contributors Analysis

(NT$ thousands) (Customer numbers)

<table>
<thead>
<tr>
<th>Year</th>
<th>Royalty</th>
<th>Customer numbers</th>
</tr>
</thead>
<tbody>
<tr>
<td>2011</td>
<td>445</td>
<td>1</td>
</tr>
<tr>
<td>2012</td>
<td>660</td>
<td>2</td>
</tr>
<tr>
<td>2013</td>
<td>1,285</td>
<td>5</td>
</tr>
<tr>
<td>2014</td>
<td>10,819</td>
<td>9</td>
</tr>
<tr>
<td>2015</td>
<td>12,232</td>
<td>15</td>
</tr>
<tr>
<td>2016</td>
<td>13,320</td>
<td>15</td>
</tr>
<tr>
<td>2017</td>
<td>38,287</td>
<td>25</td>
</tr>
<tr>
<td>2018</td>
<td>74,953</td>
<td>28</td>
</tr>
</tbody>
</table>

Driving Innovations™
2018 Top Ten Royalty Contributors
Analysis by Application

(NT$ thousands)

Top 10 Royalty Customers
Contribution: 95%

95%
5%

Touch Panel (TW)
Gaming (TW)
Touch Panel (KO)
Wireless/IoT (TW)
Navigation (CN)
Wireless display (TW)
Touch Panel (TW)
Wireless/IoT (TW)
Surveillance (TW)
Consolidated Gross Margin

Gross Profit (NT$ thousands)

<table>
<thead>
<tr>
<th></th>
<th>4Q17</th>
<th>3Q18</th>
<th>4Q18</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gross Profit</td>
<td>56,798</td>
<td>56,217</td>
<td>125,574</td>
</tr>
<tr>
<td>Gross Margin</td>
<td>99.59%</td>
<td>99.74%</td>
<td>99.96%</td>
</tr>
</tbody>
</table>

Gross Margin

<table>
<thead>
<tr>
<th></th>
<th>2017</th>
<th>2018</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gross Profit</td>
<td>288,437</td>
<td>304,340</td>
</tr>
<tr>
<td>Gross Margin</td>
<td>99.68%</td>
<td>99.86%</td>
</tr>
</tbody>
</table>
Consolidated Operating Expenses

**(NT$ thousands)**

- **4Q17**: 55,654 (R&D: 18,185, Administration: 15,991, Selling: 21,478)
- **3Q18**: 63,840 (R&D: 28,072, Administration: 14,485, Selling: 21,283)
- **4Q18**: 85,523 (R&D: 39,928, Administration: 15,138, Selling: 30,457)
- **2017**: 261,545 (R&D: 108,070, Administration: 58,416, Selling: 95,059)
- **2018**: 269,029 (R&D: 117,203, Administration: 59,834, Selling: 91,992)

YOY:
- +53.7%
- +34.0%
- +2.9%

QoQ:
- +34.0%
Consolidated Net Income

YoY +10,254%

QoQ -%

(NT$ thousands)

4Q17 3Q18 4Q18

2017 2018

QoQ +93%

YoY +93%

21,533 41,567

-10,000 -10,000

40,000 50,000

50,000

20,000

30,000

40,000

50,000

(NT$ thousands)

(6,705)

387

4Q17 3Q18 4Q18
Consolidated Operating Income

YoY: +3,401%  
QoQ: -%

(NT$ thousands)

<table>
<thead>
<tr>
<th></th>
<th>4Q17</th>
<th>3Q18</th>
<th>4Q18</th>
</tr>
</thead>
<tbody>
<tr>
<td>YoY</td>
<td>1,144</td>
<td></td>
<td>40,051</td>
</tr>
<tr>
<td>QoQ</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>YoY</td>
<td>26,892</td>
<td></td>
<td>35,311</td>
</tr>
</tbody>
</table>

(7,623)

Driving Innovations™
Consolidated Operating Margin

Year-over-Year (YoY) increase of 29.87 percentage points. Quarter-over-Quarter (QoQ) increase of 45.40 percentage points. Year-over-Year (YoY) increase of 2.30 percentage points.

Q4 2017: 2.01%  
Q3 2018: (13.52%)  
Q4 2018: 31.88%

2017: 9.29%  
2018: 11.59%
Consolidated Net Profit Margin

YoY +31.22 pt
QoQ +43.80 pt
YoY +6.20 pt

(NT$ thousands)

(11.90%)

2017 2018

13.64%
7.44%
Consolidated Earnings Per Share

<table>
<thead>
<tr>
<th>Quarter</th>
<th>4Q17</th>
<th>3Q18</th>
<th>4Q18</th>
</tr>
</thead>
<tbody>
<tr>
<td>YoY</td>
<td>+0.93</td>
<td></td>
<td></td>
</tr>
<tr>
<td>QoQ</td>
<td>+1.09</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Year</th>
<th>2017</th>
<th>2018</th>
</tr>
</thead>
<tbody>
<tr>
<td>YoY</td>
<td>+0.46</td>
<td></td>
</tr>
</tbody>
</table>

(NT$)
Revenue Analysis by Payment Model

(2018/01-12 New Agreements: 42)

- License Fee: 69%
- Running Royalty: 25%
- Service & Others: 6%

License Fee
Running Royalty
Service & Others
Revenue Analysis by Region

- **Taiwan**: 47%
- **China**: 32%
- **Korea**: 8%
- **USA**: 8%
- **Japan**: 3%
- **Europe**: 2%

(Tabulation of regional revenue percentages)
Customer Application Analysis

- IoT: 29%
- Artificial Intelligence: 19%
- Storage: 14%
- Sensing: 7%
- Networking: 7%
- Navigation: 5%
- Others: 10%
- Automotive: 9%

*Based on agreement number
Revenue Analysis by Product

- **V3**: 29%
- **RISC-V**: 71%

- **N9**: 22%
- **N10**: 13%
- **N8**: 11%
- **D10**: 8%
- **D15**: 6%
- **N13**: 4%
- **S8**: 1%
- **N7**: 3%
- **N15**: 21%
- **Platform IP, Others**: 5%
- **N25**: 3%
- **A25**: 2%
- **AX25**: 1%
- **NX25**: 1%
2018 Revenue Analysis - RISC-V

(NT$ thousands)

1Q18: 30,305 (V3: 4,376, RISC-V: 25,929)
2Q18: 64,229 (V3: 23,857, RISC-V: 40,372)
3Q18: 30,199 (V3: 26,166, RISC-V: 4,033)
4Q18: 90,918 (V3: 34,706, RISC-V: 56,212)

Percentage: 
- 1Q18: 12.6% (V3: 4,376, RISC-V: 25,929)
- 2Q18: 27.1% (V3: 23,857, RISC-V: 40,372)
- 3Q18: 46.4% (V3: 26,166, RISC-V: 4,033)
- 4Q18: 27.6% (V3: 34,706, RISC-V: 56,212)
Product Application
A 14-year-old public CPU IP company
>1B Andes-Embedded SoC shipped in 2018. >3.6B cumulatively.

A founding member of the RISC-V Foundation
A major open source maintainer/contributor
Active involvement in standard extensions
- Chair of P-extension (Packed DSP/SIMD) Task Group
- Co-chair of Fast Interrupt Task Group
Example Applications of Andes-Embedded™ SoC

- Touch Screen
- eBook/eDictionary
- Power management
- Bio-medical device
- CMMB
- MCU
- TCON

- Wireless display
- WiFi, Bluetooth
- GPS, GPON, NFC
- Gateway/router
- Portable Karaoke
- Sigfox LPWAN
- IoT Cat0 base station
- IoT MCU
- ESL
- Smart Meter
- Smart Lighting
- USB3.0
- SSD, eMMC
- Anti-virus
- Sensor Hub
- mSATA
- Secure SD
- Fingerprint Recognition

- Motor Control
- Wireless Charger
- Surveillance
- Barcode scanner
- ADAS
- VEDR
- 4K2K CODEC
- 8K4K CODEC
- and more....
IoT Application -1

- Bluetooth Speaker
- Sigfox LPWAN
- Healthcare device
- Wearable device
- Electronic price tags
- Sensor Hub
IoT Application - 2

Wearable devices

Drone

Portable Karaoke

WiFi/GPS/FM/Bluetooth combo

GPS/Beido in shared bikes

Contactless payment (NFC)
Andes Embedded in Smart Phones

1 in 5 Smart Phones are with Andes Embedded worldwide

- Sensor Hub
- NFC Controller
- WiFi/ BT/ GPS/ FM (combo)
- Storage controller
- Touch screen controller
Andes Embedded in Consumer Devices, Cars and Datacenters

- Switch: MXIC Flash Ctrl
- Echo Dot2: Mediatek WiFi IoT
- Bike Sharing: GPS Ctrl
- X-Trail: ADAS Ctrl

- In leading machine learning computers for datacenter
- In tier-one switch routers for datacenter

- Recent applications: 5G networking, 802.11ax, machine learning processors (using Andes Custom Extension, ACE)
New Products and Ecosystems
Product Lines

◆ New A-series Cores released in Andes Embedded Forum 2018

ANDES

RISC-V
Andes RISC-V Product Overview

Best extensions to RISC-V

AndeStar™ Architecture V5

AndesCore™ Processors

AndeSight™ Tools

Professional IDE with high code quality

AndeShaper™ Platforms

Handy peripheral IPs to speed up SoC construction

AndeSoft™ Stacks

Extensive SW stacks from bare metal, RTOS to Linux
V5 AndesCore™ Processors

N22
N25F/NX25F
A25/AX25
A25MP/AX25MP
Bring Andes Strength to RISC-V Core Family

- Architecture beyond the kernel for diversified requirements
- Efficient processor pipeline for leading PPA
- Platform IP support to help speed up SoC construction
- AndeSight IDE, and compiler/library optimizations
- RTOS and Linux support, and middleware (such as IoT stacks)
- Commercial-grade verification for all products
- Mass production experience with high quality deliverables
- Professional supporting infrastructure
Launch of RISC-V Core IP Series

**Cache-Coherent Multicores**

- **A25MP**
  - V5, 32b, 1-4 Cores
  - L2 Cache Coherence
  - DSP, MMU, FPU, ACE...

- **AX25MP**
  - V5, 64b, 1-4 Cores
  - L2 Cache Coherence
  - DSP, MMU, FPU, ACE...

**Linux and FPU/DSP**

- **A25**
  - V5, 32b, 5-stage, >1.2GHz, MMU/PMP, DSP, FPU, ACE...

- **AX25**
  - V5, 64b, 5-stage, >1.2GHz, MMU/PMP, DSP, FPU, ACE...

**Fast/Compact, FPU/DSP**

- **D25F: +DSP**
  - N25F
    - V5, 32b, 5-stage, >1.2GHz
    - PMP, FPU, ACE...

- **NX25F**
  - V5, 64b, 5-stage, >1.2GHz
  - PMP, FPU, ACE...

**Slim and Efficient**

- **N22**
  - V5/V5e, 32b, 2-stage
  - 800MHz, 16/32 GPR

- **D22F**
  - V5/V5e, 32b, 2-stage
  - 800MHz, 16/32 GPR, DSP, FPU

---

a. A25*MP: available Q1/2019
b. 28HPC+ RVT, SS, 0.81V, 0C, with I/O constraints.
V5 AndesCores: 25-series

- **N25F: 32-bit, NX25F: 64-bit**
  - From scratch for the best PPA
  - Very configurable

- **AndeStar V5 ISA**

- **5-stage pipeline**

- **Configurable multiplier**

- **Optional branch prediction**

- **Flexible memory subsystem**
  - I/D Local Memory (LM): to 16MB
  - I/D caches: up to 64KB, 4-way
  - Optional parity or ECC
  - Hit-under-miss caches
  - Load/store: unaligned accesses

- **N25F sample configurations @TSMC 28HPC+ RVT:**
  - Small config: 37K gates, 1.0 GHz (worst case)
  - Large config: 130K gates, 1.2GHz (worst case)
  - Best-in-class Coremark: 3.58/MHz
V5 AndesCores: 25-series

- Fast-n-small for control tasks in AR/VR, networking, storage, AI
- **N25F/NX25F**: +FPU
  - +, −, ×, ×+, ×−: pipelined 4 cycles
  - ÷, √: run in the background
    - 15 for SP, 29 for DP
  - FP load/store: support HP
- **A25/AX25**: +FP +Linux
  - Support RISC-V MMU and S-mode
  - 4 or 8-entry ITLB and DTLB
  - 4-way 32~128-entry Shared-TLB
- **Whetstone/MHz**:

![Graph showing performance metrics for N25F and competing cores](chart.png)
V5 AndesCores: 22-series

- **AndeStar V5 or V5e ISA**
  - RV32-IMC or RV32-EMC
  - Plus Andes extension

- **2-stage pipeline with AHB-lite main bus**

- **Rich baseline options:**
  - I/D Local Memory (1KB~512MB), I cache
  - Fast or small multiplier, branch predictions
  - Up to 16-entry PMP, StackSafe
  - M-mode, or M+U-mode
  - APB private peripheral port, fast IO port
  - WFI, WFE, and PowerBrake
  - Vectored and preemptive interrupt controller

- **Advanced options: ACE, DSP, FPU**

- **28nm PPA:**
  - >750 MHz (worst case)
  - <15K gates (minimal)

- **Best per-MHz performance:**
  - 1.8 DMIPS (no inline)
  - 3.97 Coremark

![Diagram of V5 AndesCores](image-url)
A(X)25MP Cache-Coherent Multicore

- 1/2/4 A25 (32-bit)/AX25 (64-bit) CPUs
  - RV-IMACFD ISA, supporting SMP Linux
  - With the latest P-extension (DSP/SIMD ISA), Andes’ contribution to RISC-V

- Hardware Multicore Cache Coherence
  - Support MESI cache coherence protocol by ACU (Andes Coherence Unit)
  - Support I/O coherence without data caches

- Level-2 Cache Controller
  - 0/128/256K...2MB, 32-byte line, 16-way
  - ECC, SECDED support

- Bus Interfaces
  - AXI bus master interface
  - Local memory slave port, for each A25/AX25 CPU
  - I/O coherence slave port
  - MP subsystem vs. bus interface synchronous N:1 clock ratio

- Platform Level Interrupt, Debug and Trace Support
ACE: Andes Custom Extension

COPilot
Custom-OPtimized Instruction development Tools

- Extended Tools
- Extended ISS
- Extended RTL

Automated Env. For Cross Checking

- Test Case Generator
- Compiler
  - Asm/Disasm
  - Debugger
  - IDE

- CPU ISS
  - (near-cycle accurate)

Extensible Baseline Components

- Executable or library
- Source file

Verilog user.v
concise RTL
semantics, operands, test-case spec
script user.ace
**Aggressive in RISC-V Community**

**Foundation Task Groups (partial list)**

- **Bit Manipulation**
- **Compliance**
- **Debug**
- **Memory Model**
- **P-Extension**
- **Privileged Spec**
- **Vector**
- **Security**
- **Base ISA/Opcode**
- **Fast Interrupts**

- Contributing hardware architecture extensions
  - Chair of the P-extension (Packed SIMD/DSP) Task Group
  - Co-chair of Fast Interrupts Task Group
  - Closely reviewing activities of other Task Groups
Andes Helps Strengthen RISC-V Ecosystem

► More choices for customers are good
► Andes works closely with partners to grow RISC-V ecosystem
RISC-V Software Ecosystem: GNU Toolchain

- GCC, binutils: May, 2017
- Newlib: Aug, 2017
- Glibc (rv64i): Feb, 2018
- GDB: Mar, 2018
- OpenOCD: July, 2018
- Glibc (rv32i):
  - Submitted in July 2018 (by Andes)
  - Review in progress

GNU Toolchains

Barcelona
May 2018

LLVM

Linux
RISC-V Software Ecosystem: LLVM Compilation

- **LLVM:**
  - RV32IMAFDC: June, 2018
  - Relaxation: May, 2018 (by Andes)
  - 64b support: Nov, 2018
  - Missing hard-float calling convention

- **compiler-rt:** Mar, 2018

- **LLD:** Aug, 2018 (by Andes)
  - Initial port (relocation and TLS) in Oct. 2017
  - Dynamic linking review in progress since Oct, 2017
  - Missing link-time relaxation
RISC-V System Software Ecosystem: Linux

- **U-boot**: Jan, 2018 (by Andes)
- **Kernel (rv64i)**: Jan, 2018
- **Key utilities**: (by Andes)
  - Perf: Feb, 2018
  - Kernel Module: May, 2018
  - Ftrace: May, 2018
- **Kernel (rv32i)**: Jun, 2018 (by Andes)
- **Kernel with CONFIG_FPU**: Oct, 2018 (by Andes)
Andes Position in RISC-V

Complete product portfolio

Reliable RISC-V core IP provider

RISC-V cores that run Linux

Extreme low power consumption, high computing efficiency

World’s leading Customer-Extension Capable RISC-V Core
2018 RISC-V Design Win

Sixteen design wins for Andes RISC-V Core IPS:
- NX25: Enterprise SSD (Taiwan)
- N25: AI (China w/ ACE), Blockchain (China), HD-PLC (Japan), SSD (China), Fingerprint (Taiwan), AI (China x2), TDDI (Taiwan), SD/eMMC (Taiwan), Research/Academic (Taiwan x2)
- N25/AX25: FPGA for AI (US)
- AX25: FPGA for AI (China)
- A25: 5G (US), Automotive (Korea)

Thirteen design service providers joined Andes RISC-V Easy Start Program:
- US x 3, Europe x1, Korea x 1, China x 3, Taiwan x 5
## Summary of AndesCores vs. Competitors

<table>
<thead>
<tr>
<th>AndesCore™</th>
<th>AndesCore/Competitor Power Efficiency&lt;sup&gt;1&lt;/sup&gt; (DMIPS/mW)</th>
<th>Competitors</th>
</tr>
</thead>
<tbody>
<tr>
<td>N7</td>
<td>+42%</td>
<td>Cortex-M0+</td>
</tr>
<tr>
<td>N8</td>
<td>+43%</td>
<td>Cortex-M3</td>
</tr>
<tr>
<td>N9</td>
<td>+43%</td>
<td>Cortex-M3</td>
</tr>
<tr>
<td>D10</td>
<td>+48%</td>
<td>Cortex-M4</td>
</tr>
<tr>
<td>N13</td>
<td>+185%</td>
<td>Cortex-A5</td>
</tr>
<tr>
<td>N13</td>
<td>+45%</td>
<td>Cortex-R4</td>
</tr>
<tr>
<td>D15F</td>
<td>+121%</td>
<td>Cortex-M7</td>
</tr>
</tbody>
</table>

1. Power Efficiency is DMIPS/MHz divided by power consumption (mW/MHz) when running Dhrystone.
Two Ecosystems: Andes and Knect.me
Built up Ecosystem *knect.me* to help IoT Developing
- to *knect* solutions - Silicon IP’s, SW stacks, tools, applications, systems and products

Includes:
- SoC IP Platforms
- Software Stack
- Development Boards
- Development Tools

To Form a IoT League
- to *knect* chip vendors, partners, application developers, system vendors
Andes Awarded
Leader of the Emerging Technology

“2018 Top25 emerging tech solutions provider”
— CIO Advisor Magazine
Concluding Remarks
Andes revealed new RISC-V processor cores (N22, A(X)25MP, D25F) to fit in more applications from customers.

Andes aggressively involved in RISC-V Foundation new technology development, contributing and leveraging RISC-V eco-system.

Andes has successively signed thirteen contracts with design service houses in 2018 to authorize ASIC design to embed RISC-V core (Andes RISC-V Easy Start Program). Andes aim to sign up 20 design service houses worldwide in a few months. These contracts will create a win-win situation for Andes, design service houses and customers.
Thank You!

www.andestech.com
Q&A
AndeStar™ V5: New Generation of ISA Kernel

Full Feature

Baseline

RISC-V Kernel

CoDense™
StackSafe™
PowerBrake

Custom Ext.
DSP/FP Ext.
Security Ext.

Compiler Opt.
>200 DSP Libraries
COPILLOT tools
Secure RTOS

RV32/64IMACFD+Andes Ext.