The Next Generation RISC-V Processors
AndesCore™ 27, 45 Series

Jason Lin & KY Hsieh
Sr. Technical Marketing Managers
Marketing Division
2020/05/07
Agenda

- Andes V5 Processor Lineup
- 27-Series
  - Overview
  - MemBoost for High Performance Memory Subsystem
- 45-Series
  - Overview
  - Performance & Speedup
  - Lineup
- Target Applications of 27&45-Series
- Summary
# Andes Corporate Overview

**Silicon Valley Tie**
- Core R&D from AMD, DEC, Intel, MIPS, nVidia, and Sun

**15-Year CPU IP Company**
- IPO in 2017; HQ in Taiwan
- AndeStar™ V1-V3, V5 (RISC-V)

**>1 Bn Annual Run Rate of Andes-Embedded SoC**
- ~300 customers in TW, CN, US, EU, JP, KR

**Founding Platinum Member and Major Contributor**
- Chairing Task Groups
- Contributing to GNU, LLVM, uBoot, glibc, Linux, etc.
### Andes V5 Processor Lineup

<table>
<thead>
<tr>
<th>Feature</th>
<th>RV32</th>
<th>RV64</th>
<th>Vector Ext.</th>
<th>Superscalar</th>
</tr>
</thead>
<tbody>
<tr>
<td>Linux with FPU/DSP</td>
<td>A25</td>
<td>AX25</td>
<td>A27/AX27 and more.</td>
<td>N45/NX45, D45/DX45, N45/NX45, A45/AX45</td>
</tr>
<tr>
<td>Fast/Compact with FPU/DSP</td>
<td>N25F</td>
<td>NX25F</td>
<td>5-stage (1.1 GHz)</td>
<td>8-stage (1.2 GHz)</td>
</tr>
<tr>
<td></td>
<td>D25F</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Note:** Common features are RV*IMACN, Caches, LM, ECC, BrPred, CoDense™, PowerBrake, StackSafe™, ACE (Andes Custom Extension™); Frequencies at 28nm

2020 RISC-V CON Webinar
Andes 27-Series
RISC-V CPU IP Cores
AndesCore™ 27 Series

**A27 and AX27**
- RV*GC-N-P
- 5-stage single-issue
- Programmable PMA table
  - PMA: Physical Memory Attribute
- Leveraging the mature 25-series; so same scalar performance

**MemBoost**
- Skip unnecessary writes to dcache
- Multiple outstanding data accesses
- I/D cache prefetch
- Memory performance\(^1\) over 25-series:
  - 230% higher bandwidth
  - 25-50% lower latency

Note 1: measured by popular benchmark Tinymembench

---

**27-series uCore, PMP**

Note 1: measured by popular benchmark Tinymembench
MemBoost - Enhanced Memory Performance

- **Data Cache Write-Around**
  - Smart cache line allocation policy, for better cache utilization and reduce number of memory accesses

- **Instruction and Data Pre-fetch**
  - Conditionally fill instruction and data caches in advance, for minimum memory access latency

---

**Diagram Details:**

- **CPU Core**
  - Data Cache
  - Instruction and Data Cache

- **Main Memory**
  - Read/Write allocates to cache line
  - The cache line is evicted later
  - Write-around reduces memory accesses

- **Next instruction line fetch**
- **Data streaming fetch**
MemBoost - Enhanced Memory Performance

- **Multiple Outstanding Mem. Req.**
  - Issue multiple transactions to data memory sub-system for higher bus utilization, also support out-of-order completion

- **Dedicated I & D Bus Interfaces**
  - Separate instruction and data buses, for instruction and data’s own memory transactions

- **Multiple Requests Support Out-of-Order Completion**

- **Expanded memory bandwidth**

- **Support Out-of-Order Completion**

2020 RISC-V CON Webinar
An Example of Multi CPU System

- Organization for many single cores

- Separated Instruction and Data Bus Option
  - Enable efficient memory sub-system design

- Uncached Regions by PMA
  - Can be used to communicate data among cores

- CCTL Cache Control
  - Cache lines invalidate, write-back, fill, lock... operations
Andes 45-Series Superscalar RISC-V CPU IP Cores
AndesCore™ 45 Series Overview

- 8-stage in-order dual-issue
- AndeStar™ V5 ISA:
  - RV*GCN (S/D FPU)
  - RV*P-ext (DSP/SIMD)
  - MMU: for Linux Applications
  - ALL have Andes extensions
- Dual-issue most instruction pairs
  - Except for 2 MUL/FPU/DSP/LD_ST and some special dependent ALU instruction pairs
  - Late ALUs enable 0-cycle load-use penalty
- MemBoost for memory subsystem
- Low power dynamic branch prediction
- Unaligned data accesses
- Fast or small multiplier

Note: 2nd cycle of $/LM is for alignment
45-Series: Features

- Virtual memory support:
  - Shared TLB: 32-512 entries
  - ITLB/DTLB: 4 or 8 entries

- Physical memory support:
  - Physical Memory Protection (PMP): 16 regions
  - Programmable Physical Memory Attribute (PMA): 16 regions

- VA/PA address bits

<table>
<thead>
<tr>
<th>VA modes</th>
<th>No MMU</th>
<th>SV32</th>
<th>SV39</th>
<th>SV48</th>
</tr>
</thead>
<tbody>
<tr>
<td>PA bits</td>
<td>RV32</td>
<td>32</td>
<td>34</td>
<td>--</td>
</tr>
<tr>
<td></td>
<td>RV64</td>
<td>32-64</td>
<td>--</td>
<td>38</td>
</tr>
</tbody>
</table>

- Privilege modes:
  - Machine/User modes
  - Optional Supervisor mode
45-Series: Features

**L1 I/D Caches:**
- Size: 8KB to 64KB
- Cache line size: 64B
- 2-way or 4-way set associative
- Optional Parity or ECC error protection

**I/D Local Memory (ILM/DLM):**
- 4KB up to 16MB
- SRAM interface support
- Slave port accesses from bus masters
- Optional Parity or ECC error protection
45-Series: Features

- **MemBoost:**
  - Instruction and data prefetch
  - Non-blocking loads/stores
    - Multiple outstanding bus requests
    - Out-of-order transaction completion
    - Allow SW-controlled prefetch
  - Data cache write-around
  - Optional separated BIU I/D buses
45-Series: Features

- **Platform-Level Interrupt Controller (PLIC)**
  - 1023 interrupt sources
  - 255 interrupt priorities
  - 16 PLIC interrupt targets
  - Enhanced interrupt features
    - Vectored interrupt dispatch
    - Priority-based preemption
    - Selectable edge trigger or level trigger

- **Bus Interfaces**
  - AXI 64-bit master port
  - Synchronous N:1 core vs. bus clock ratio
45-Series: Features

- **Debug:**
  - Up to 8 triggers per core
  - Exception redirection handling
  - 2 wires and 4 wires

- **CoDense™:**
  - Code compression technology on top of RISC-V C-extension

- **Power Management**
  - **QuickNap™**
    - Logic power-down and SRAM in retention
    - Put dirty bits in tag SRAM instead of flops
    - Eliminate the need to flush data cache
  - PowerBrake
    - Digitally adjust power (via stalling pipeline)
  - WFI (Wait For Interrupt)

- **StackSafe™**
  - HW stack protection
  - Protect stack from over/underflow
Target frequency (worst case): ≥1.2 GHz @28HPC+

Benchmark performance

- **Coremark**
  - N45: 5.40 (per MHz)
  - NX45: 5.38 (per MHz)

- **DMIPS (no-inline)**
  - N45: 2.89
  - NX45: 3.14

- **Embench-IOT (v0.5)**
  - N45: 2.68
  - NX45: 2.77

~50% faster than single-issue 25-Series (per-MHz)
45-Series Lineup

- **NX45**
  - 64bit Baseline
  - RV64 GCN
  - High Performance Embedded System

- **N45**
  - 32bit Baseline
  - RV32 GCN
  - High Performance Embedded System

- **DX45**
  - Baseline + P-ext* (DSP/SIMD)

- **D45**
  - Baseline + P-ext* (DSP/SIMD)
  - High Performance with DSP/SIMD

- **AX45**
  - RV64GCNP + MMU

- **A45**
  - RV32GCNP + MMU
  - Application Processor
  - Linux capable

* : RV-P is draft

All available at Q3/’20

**G: IMAFD**

2020 RISC-V CON Webinar
Target Applications of 27&45-Series

- AI/Deep Learning
- AR/VR
- 5G
- Networking
- Storage
- Video Surveillance
- ADAS
- V2X (Vehicle to Everything)
- IVI (In-Vehicle-Infotainment)

... And more!
Summary

27&45-Series Extend Andes Success from Edge to Cloud!

Performance & Extensibility
- Leading PPA and code size
- Rich data processing in P, V, and ACE

Configurability
- Flexible configurations for rich features

Maturity
- Compiler optimizations, and SW stacks
- Comprehensive features in AndeSight IDE
Thank you,
See you next webinar!