Andes Custom Extension™ Feature Extended on Menta eFPGA for RISC-V Cores ISA Reconfigurability

RISC-V CON China

August 2021

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AGENDA

1. Menta Corporate Overview
2. Partnership Overview
3. Reconfiguration Customized Instructions in Andes RISC-V Core

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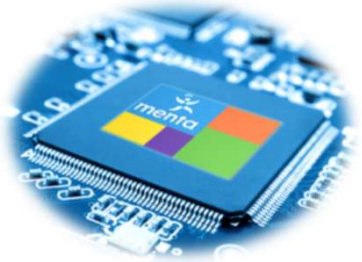
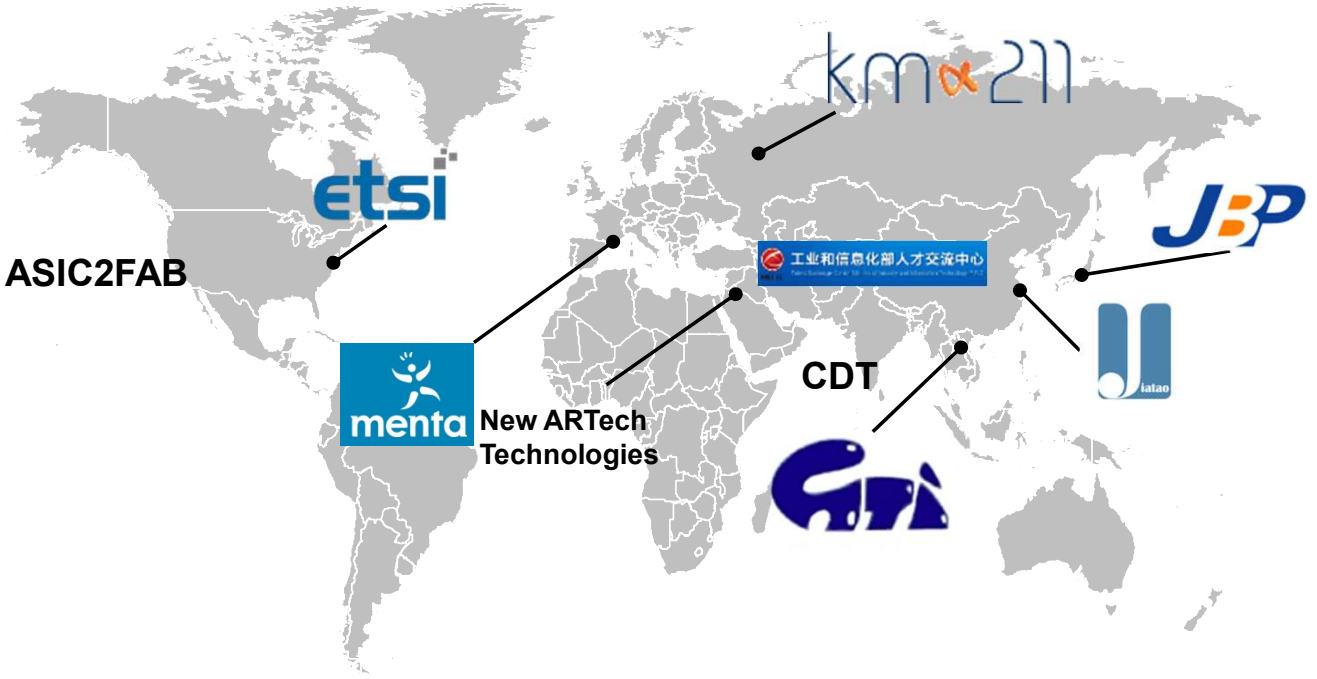
Corporate

13+ years of R&D



Patented third party standard cells IP



HQ and R&D: Sophia-Antipolis, France

Sales representatives & Business Development in China (incl. Taiwan), Israel, Japan, North America and Russia

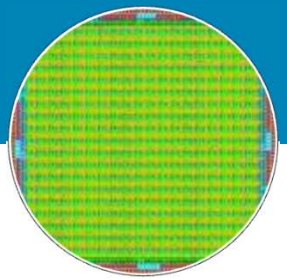
Menta eFPGA IP: from FPGA to ASIC mindset

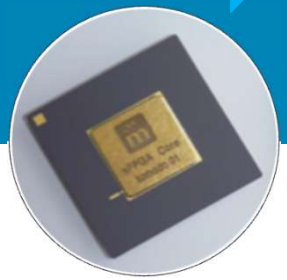
menta

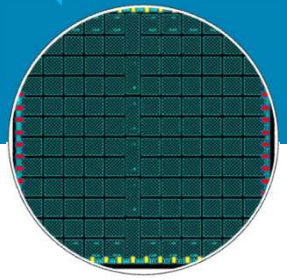
ANDES TECHNOLOGY

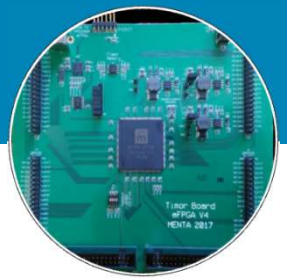
FPGA mindset

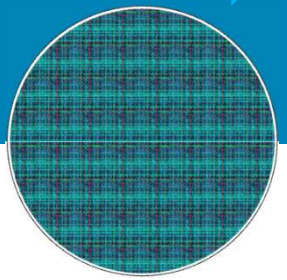
ASIC/SoC mindset







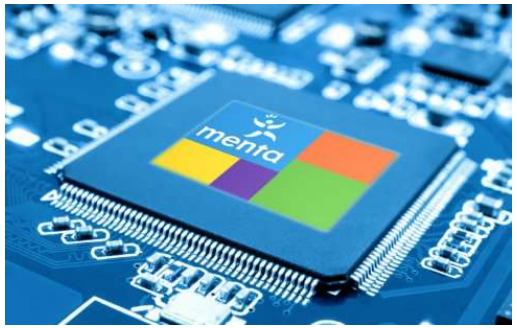




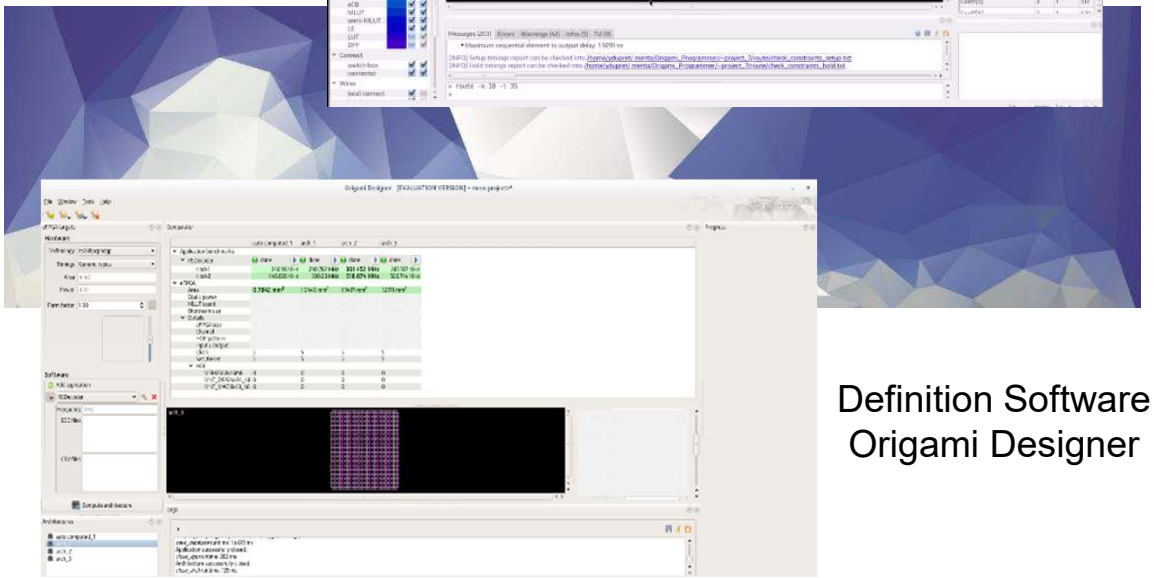
2007	2009	2011	2013	2015	2016	2018
	v1 Custom design SRAM based LUT4 based STM 65nm	**v1 MRAM** Custom design MRAM based LUT4 based STM 130nm	**v2** Custom design SRAM based LUT6 based STM 65nm	**v3** Digital design DFF based LUT6 based GF14LPP	**v4** Digital design DFF based LUT6 based TSMC28HPC+	**v5** Digital design DFF based LUT6 based Many foundries
		World 1st	EUROPEAN DEFENCE AGENCY	Any process Scan chain DfT …	+20% density performances Power consumption	+50% density performances Power consumption

Menta Products

Combine ASIC/SoC and FPGA



Programming
Software
Origami Programmer



Definition Software
Origami Designer

Enable SoC lifetime re-programmability

Mentor® A Siemens Business

Unified Software Platform

Define the perfect eFPGA IP

Supported Silicon Technology

Digital IP – we support **any** CMOS Foundry and Node

From 350nm to 5nm and less

GLOBALFOUNDRIES	STM	TSMC	XFAB
32 SOI*	130	28 HPC+	XH018
22FDX**	65LP	12FFC	
12LP*	28 FDSOI		

* Qualified

** Menta is a FDX'celerator partner

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Partnership Overview

Menta and Andes Announce Partnership Enabling Hardware Reconfiguring for ISA Extension:
https://www.globenewswire.com/fr/news-release/2020/12/07/2140834/0/en/Menta-and-Andes-Announce-Partnership-Enabling-Hardware-Reconfiguring-for-ISA-Extension.html

- Enable embedded programmable logic through Menta eFPGA in RISC-V AndesCore™ families

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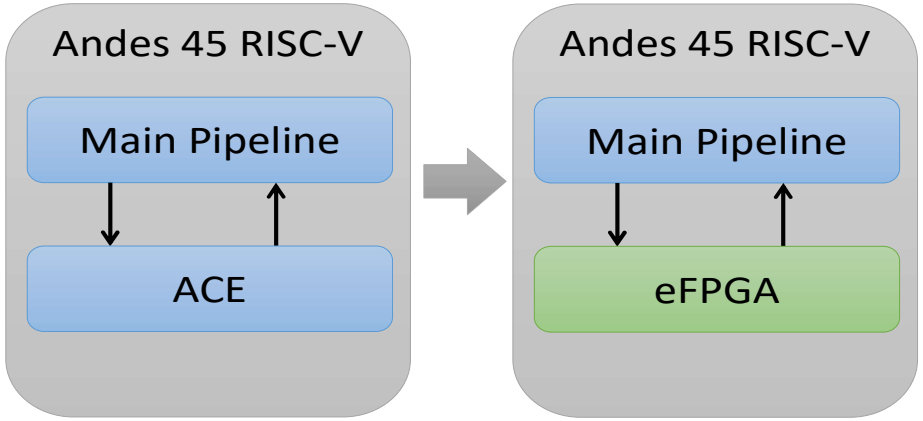
- Menta and Andes share the same vision, providing customers with a joint solution that allows customized instruction set architecture (ISA) extensions to be added or changed in the field.

- Ability to add any custom instruction needed for the function that we want to accelerate, in the field

- Does not break any software compatibility and leaves space for development and differentiation



Before Tapeout
RTL Level

After Tapeout
Harden Subsystem

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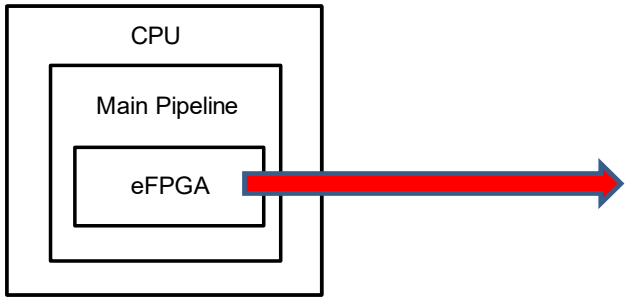
Reconfiguration Customized Instructions in Andes RISC-V Core

eFPGA Co-Extended CPU subsystem hardware extension

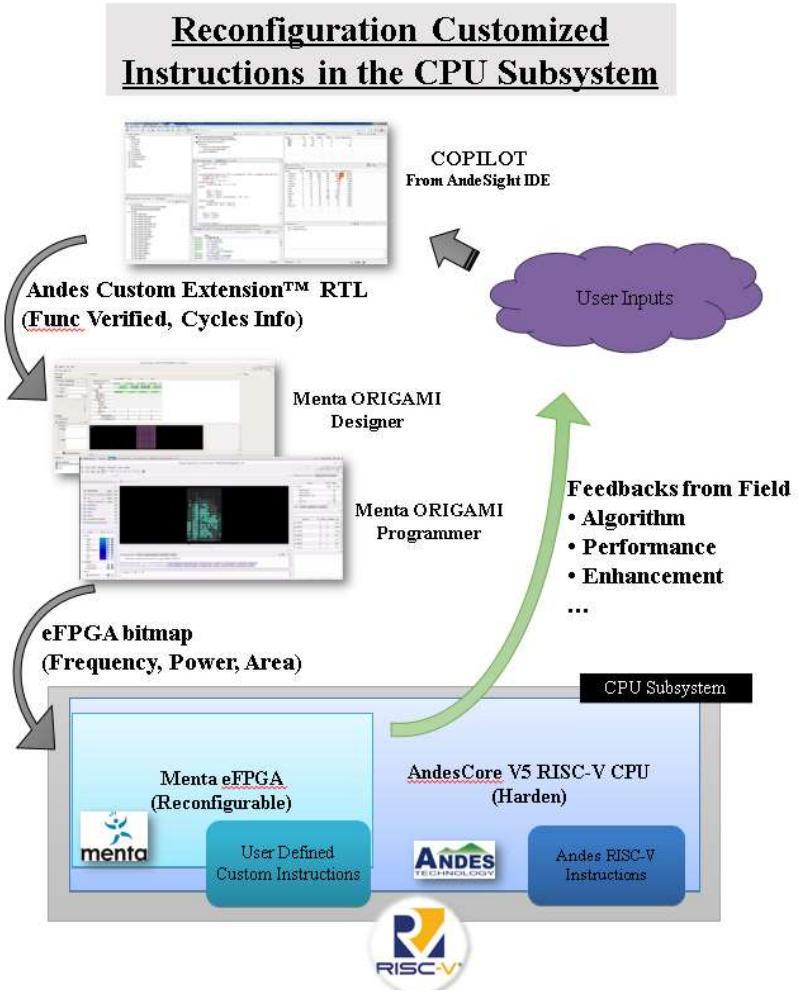
Menta eFPGA core integrated with 45-series RISC-V processor, being part of the 45-series RISC-V extended microarchitecture.



The eFPGA IP is implementing all the ACE features.

Such subsystem architecture enables customized ISA extensions and instructions with reconfigurability in the field, giving to the end user, more freedom and less risk to innovate.

Reconfiguration Customized Instructions in Andes RISC-V Core



Solution provided with a Software Development Package (SDK):

- Tools for developing on Menta eFPGA and Andes processors
- Pre-built libraries that customer can use without having to rebuild himself
- And documentation explaining how all of these pieces work together.

谢谢

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