



RISC-V CON

ONLINE WEBINAR

晶心科技

RISC-V 軟體解決方案

解決方案架構工程處
沈智明

Andes Corporate Overview



Silicon Valley Tie

- Core R&D from AMD, DEC, Intel, MIPS, nVidia, and Sun

15-Year CPU IP Company

- IPO in 2017; HQ in Taiwan
- AndeStar™ V1-V3, V5 (RISC-V)

>1 Bn Annual Run Rate of Andes-Embedded SoC

- ~300 customers in TW, CN, US, EU, JP, KR

Founding Platinum Member and Major Contributor

- Chairing Task Groups
- Contributing to GNU, LLVM, uBoot, glibc, Linux, etc.



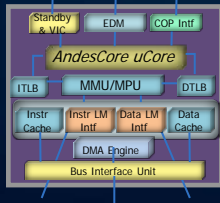
Andes V5 Product Overview

Best extensions to RISC-V

AndeStar™ Architecture V5

Highly optimized design with leading PPA

AndesCore™ Processors



Handy peripheral IPs to speed up SoC construction



AndeShape™ Platforms

AndeSight™ Tools

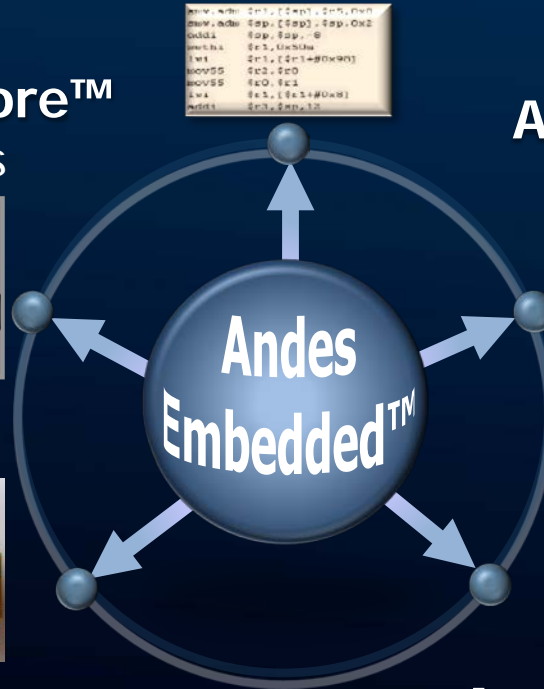
Professional IDE with high code quality



Extensive SW stacks from bare metal, RTOS to Linux



AndeSoft™ Stacks



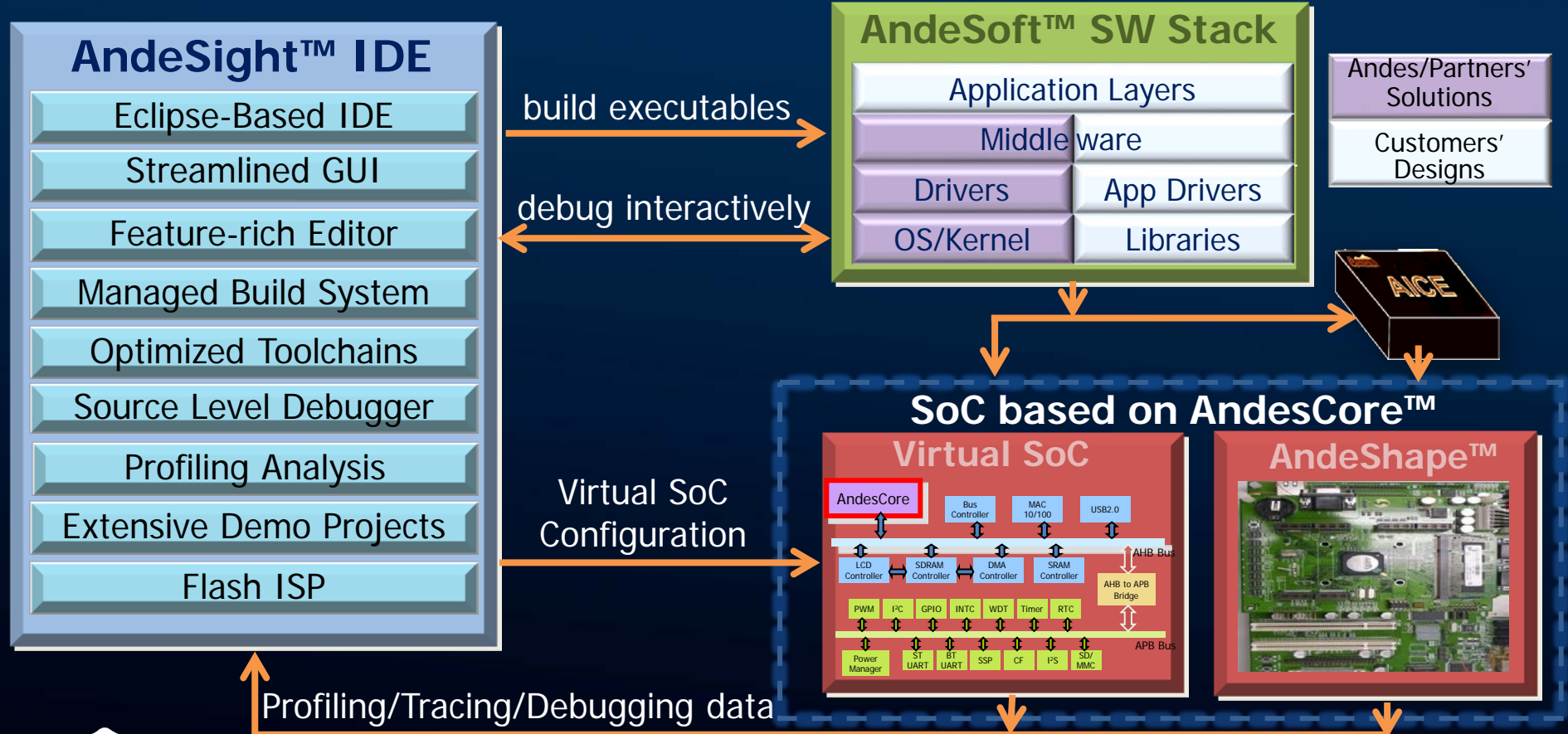
```
new, add: 0x1, 0x0, 0x0, 0x0
new, add: 0x0, 0x0, 0x0, 0x0
addi: 0x0, 0x0, 0x0
sw: 0x0, 0x0, 0x0
sw: 0x0, 0x0, 0x0
sw: 0x0, 0x0, 0x0
sw: 0x0, 0x0, 0x0
sw: 0x0, 0x0, 0x0
sw: 0x0, 0x0, 0x0
sw: 0x0, 0x0, 0x0
```



Agenda

- Overview of Tools and Runtime Support
- AndeSight™ IDE: Simulator, Compilation and debugging
- AndeSoft™ BSP: Bare Metal, RTOS, Linux and DSP ISA
- Summary

SoC SW Development Environment



Overview of Tools and Runtime Support

■ AndeSight™ IDE

- **Simulator:** AndeSim (near-cycle accuracy), Qemu
- **Compilation:** GNU toolchain, LLVM compiler/linker, optimized MCU library, DSP library
- **Debugging:** GDB, speed-optimized OpenOCD, USB-to-JTAG ICE cable



■ AndeSoft™ BSP

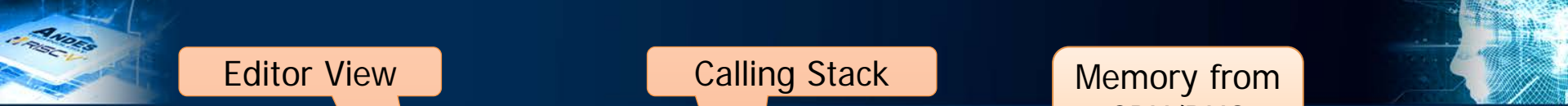
- Several Bare metal sample projects for Andes-specific features
- **RTOS:** FreeRTOS, Zephyr, LiteOS, RT-Thread
- **Linux:** MMU/TLB support, LTP tested
- Arduino support for Andes Corvette-F1 FPGA board





AndeSight™ IDE

Comprehensive Development Environment



Editor View

Calling Stack

Memory from
CPU/BUS

Project
Explorer

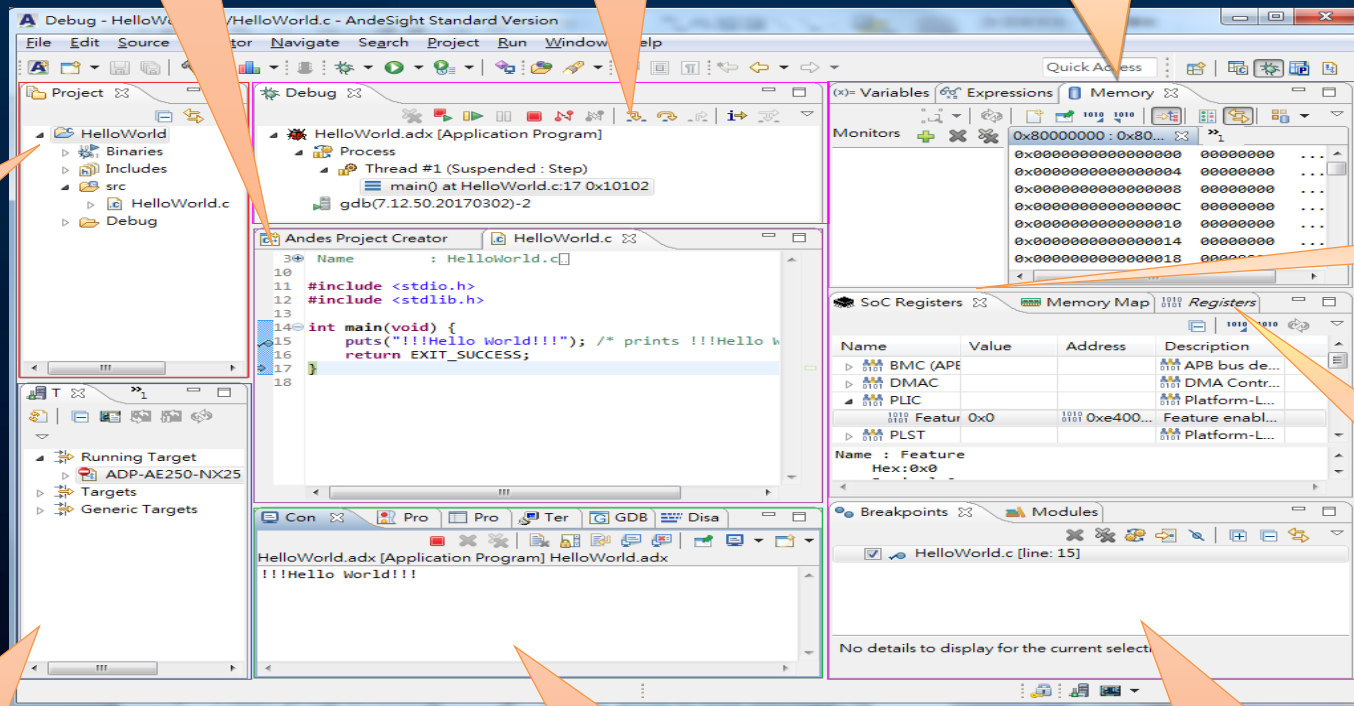
SoC Register

CPU Register

Target Manager

Console

Breakpoint



AndeSight™: Professional IDE

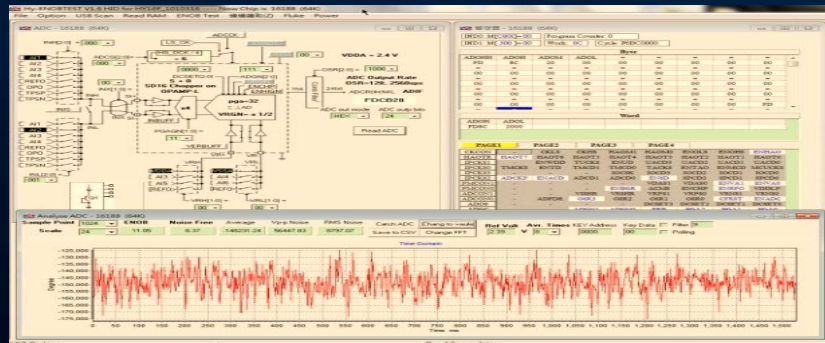
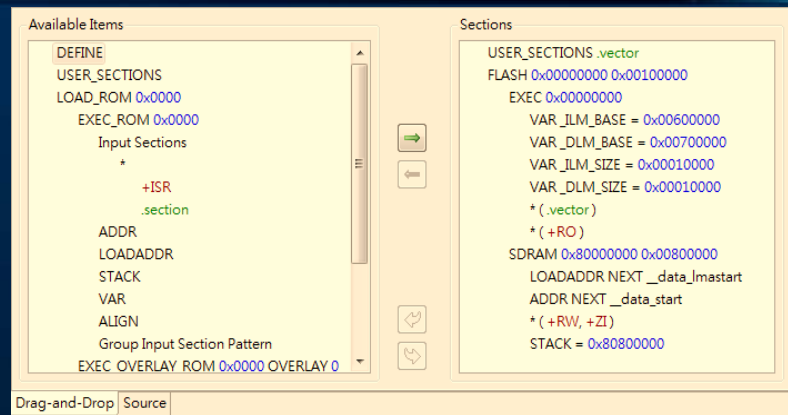
■ Project Setup:

- Meta linker script editor
- Flash ISP configured through GUI

■ Debug Support:

- Virtual hosting
- Register Bitfield display/update
- Break-n-Display on exceptions
- Script-Based RTOS awareness
- Stack protection handling

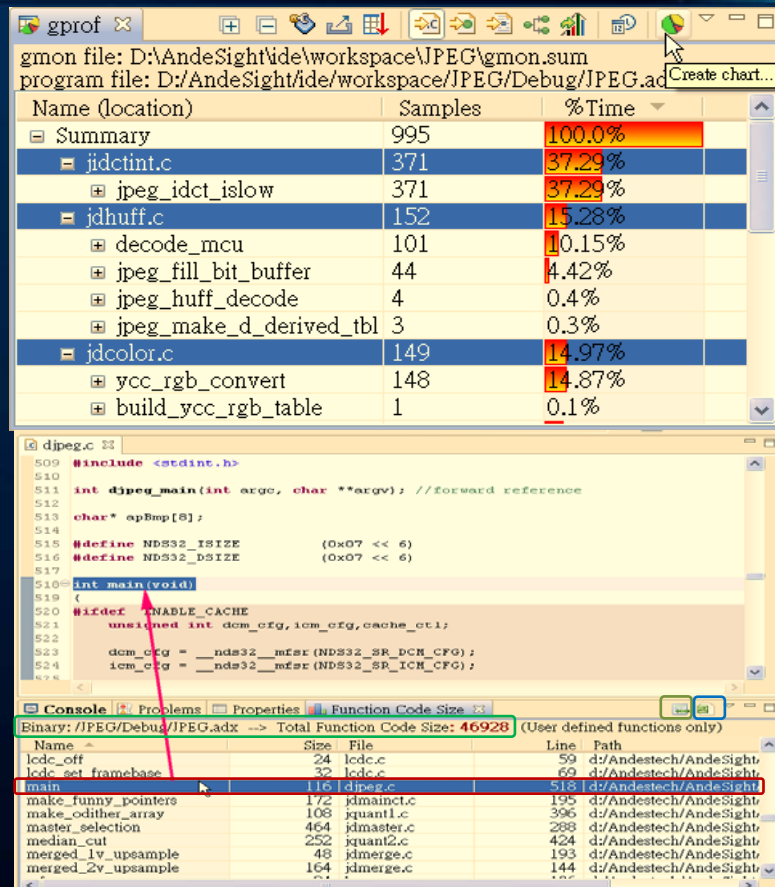
■ Custom Plugin Interface



AndeSight™: Profiling

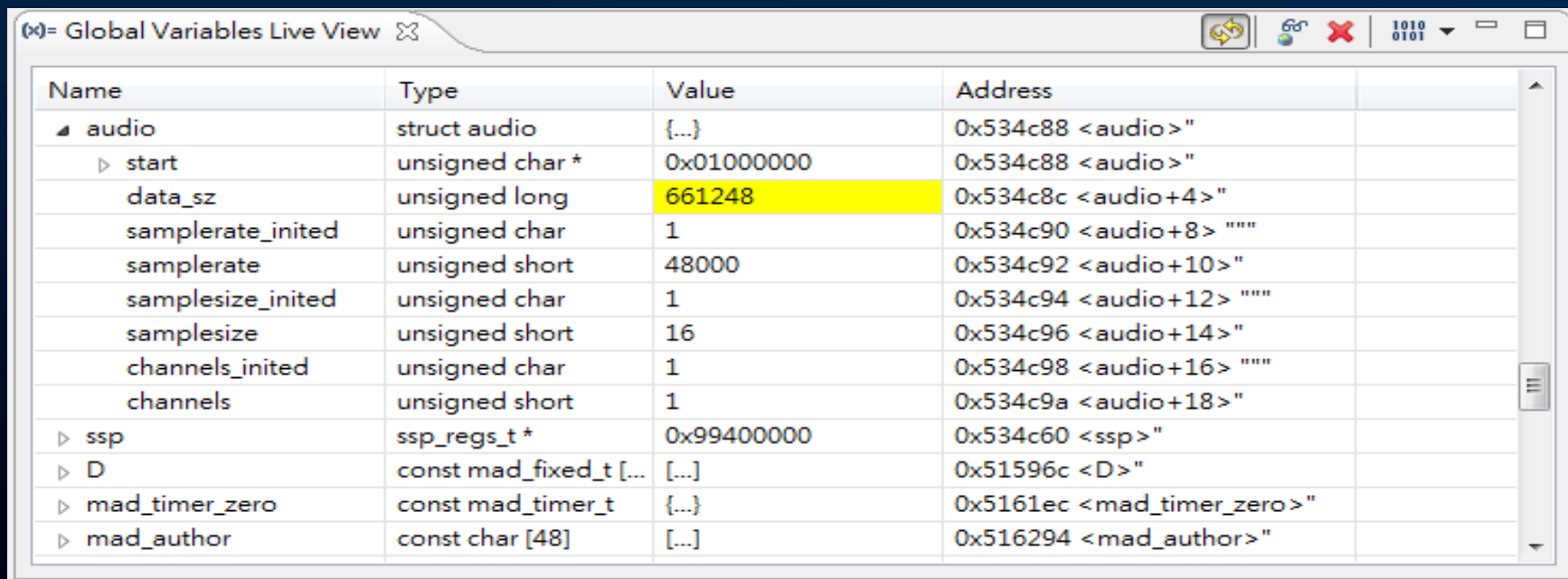
■ Program Analysis

- Function Profiling
- Code Coverage
- Performance Meter
- Function Code Size
- (Static) Stack Size



Global Variables Live View

- Runtime updating global variables in a fixed interval
- Highlight the changings in yellow



The screenshot shows a window titled "Global Variables Live View" with a table of global variables. The table has four columns: Name, Type, Value, and Address. The 'data_sz' variable is highlighted in yellow, indicating a change. The table lists variables for an audio struct, ssp, and mad modules.

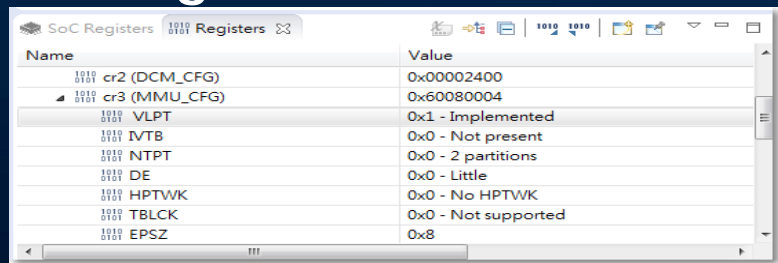
Name	Type	Value	Address
audio	struct audio	{...}	0x534c88 <audio>"
▶ start	unsigned char *	0x01000000	0x534c88 <audio>"
data_sz	unsigned long	661248	0x534c8c <audio+4>"
samplerate_initd	unsigned char	1	0x534c90 <audio+8> ""
samplerate	unsigned short	48000	0x534c92 <audio+10>"
samplesize_initd	unsigned char	1	0x534c94 <audio+12> ""
samplesize	unsigned short	16	0x534c96 <audio+14>"
channels_initd	unsigned char	1	0x534c98 <audio+16> ""
channels	unsigned short	1	0x534c9a <audio+18>"
▶ ssp	ssp_regs_t *	0x99400000	0x534c60 <ssp>"
▶ D	const mad_fixed_t [...]	[...]	0x51596c <D>"
▶ mad_timer_zero	const mad_timer_t	{...}	0x5161ec <mad_timer_zero>"
▶ mad_author	const char [48]	[...]	0x516294 <mad_author>"

Register Bitfield Viewing and Update

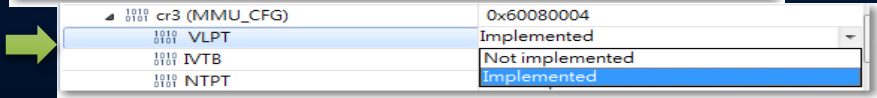
■ Bit Fields Display and Update

- CPU registers
- SoC registers

■ CPU registers



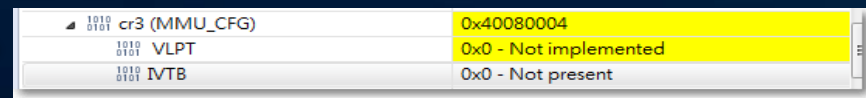
Name	Value
cr2 (DCM_CFG)	0x00002400
cr3 (MMU_CFG)	0x60080004
VLPT	0x1 - Implemented
IVTB	0x0 - Not present
NTPT	0x0 - 2 partitions
DE	0x0 - Little
HPTWK	0x0 - No HPTWK
TBLCK	0x0 - Not supported
EPSZ	0x8



cr3 (MMU_CFG)	0x60080004
VLPT	Implemented
IVTB	Not implemented
NTPT	Implemented

■ Benefits

- Bit fields can be modified at runtime
- Description of Bit fields can be shown
- Good for debugging and programming

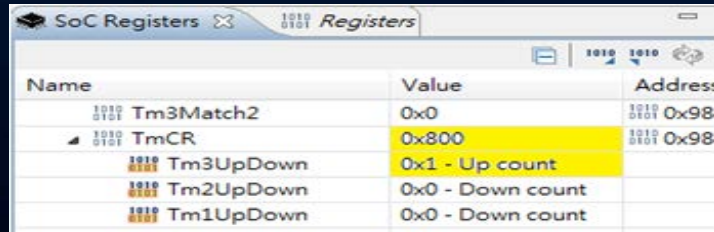


cr3 (MMU_CFG)	0x40080004
VLPT	0x0 - Not implemented
IVTB	0x0 - Not present

■ SoC registers



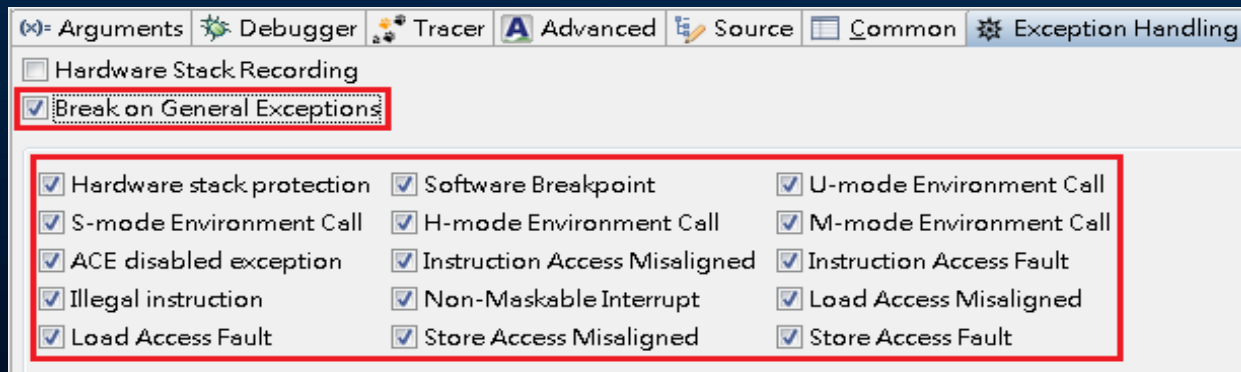
Name	Value	Address
Tm3Match2	0x0	0x98...
TmCR	0x0	0x98...
Tm3UpDown	0x0 - Down count	
Tm2UpDown	0x0 - Down count	
Tm1UpDown	0x1 - Up count	



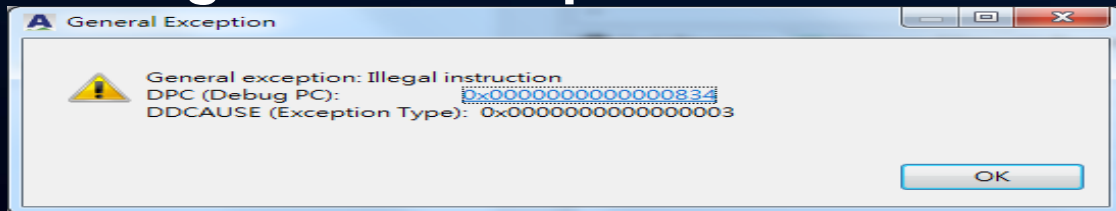
Name	Value	Address
Tm3Match2	0x0	0x98...
TmCR	0x800	0x98...
Tm3UpDown	0x1 - Up count	
Tm2UpDown	0x0 - Down count	
Tm1UpDown	0x0 - Down count	

General Exception Handling

- It helps user to catch the root cause with ease
 - No need to modify the source code
- IDE debug configurations setting:



- When general exception is raised, it will pop up an error



Script-Based RTOS Awareness

- Provide RTOS information to help debugging
- Display contents controlled by a Python script

task name	number	priority	start of stack	top of stack	status
[-] "IDLE"	3	0	0x208438 <uxIdleTaskStack.2447>	0x208af0 <...	Running
[-] "Task 2"	2	2	0x200cf8 <ucHeap+2272>	0x2013d0 <...	Delayed
[-] "Task 1"	1	1	0x200430 <ucHeap+24>	0x200b08 <...	Delayed
[-] "Tmr Svc"	4	6	0x208c38 <uxTimerTaskStack.2454>	0x209ac0 <...	Suspended

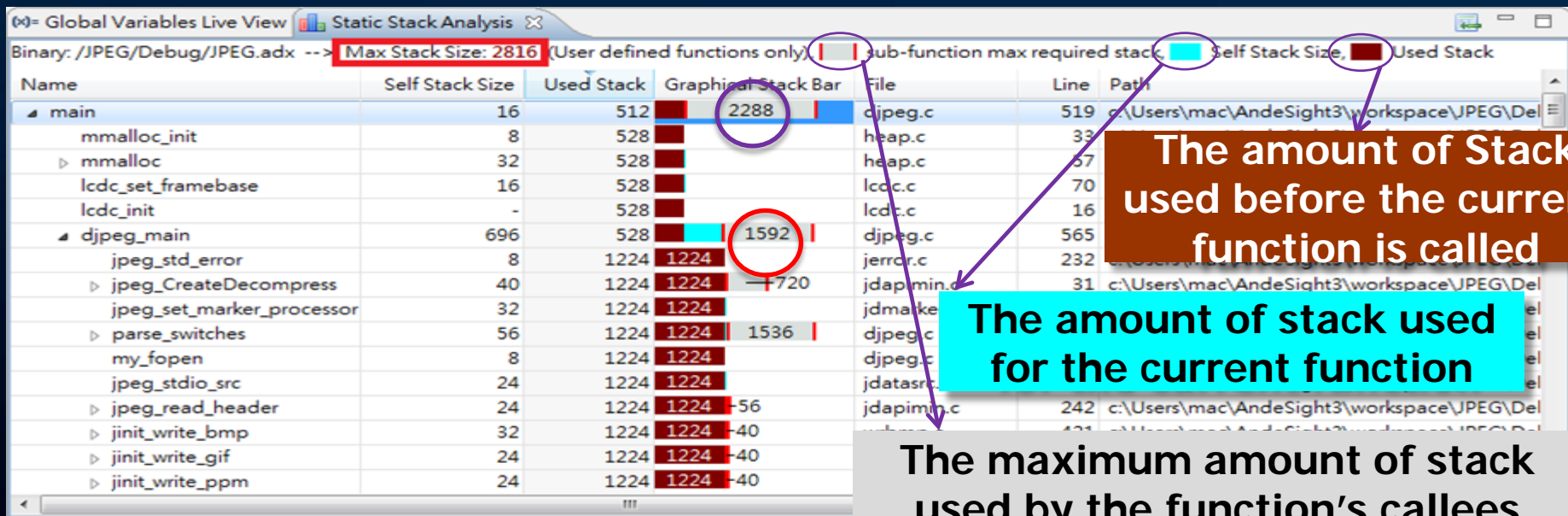
Registers			
\$x1	\$x2	\$x3	\$x4
0x00003d4a	0x002073b0	0x00200900	0x00000000
\$x5	\$x6	\$x7	\$x8
0x00000000	0x00000001	0x7ea0c49a	0x0000000a
\$x9	\$x10	\$x11	\$x12
0x0020bd08	0x00000000	0x40520000	0x00000000
\$x13	\$x14	\$x15	\$x16
0x402b0000	0x80a40000	0x40500000	0x00000000
\$x17	\$x18	\$x19	\$x20
0x000007fe	0x0020bcc0	0x7fffffff	0x00000000

queue name	handler address	max length	item size	messages waiting
[-] "TmrQ"	0x200378	5	32	0
[-] task name	number			
"Tmr Svc"	4			



Static Stack Analysis View

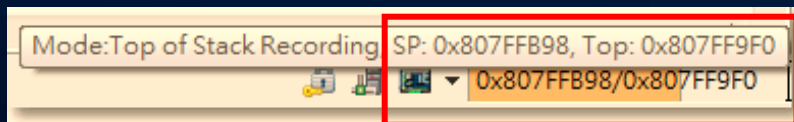
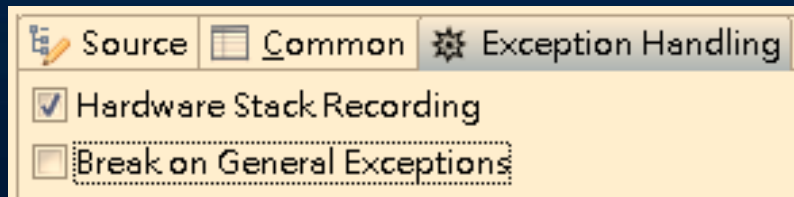
- Sizes estimated statically after project is built
- Report the maximum stack size of the whole program
- Display information of stack usage for each function



StackSafe™ Protection Handling

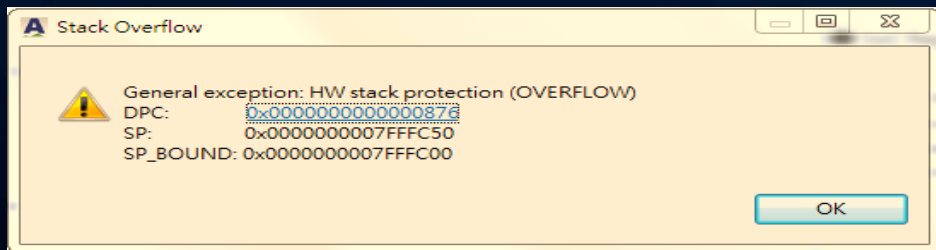
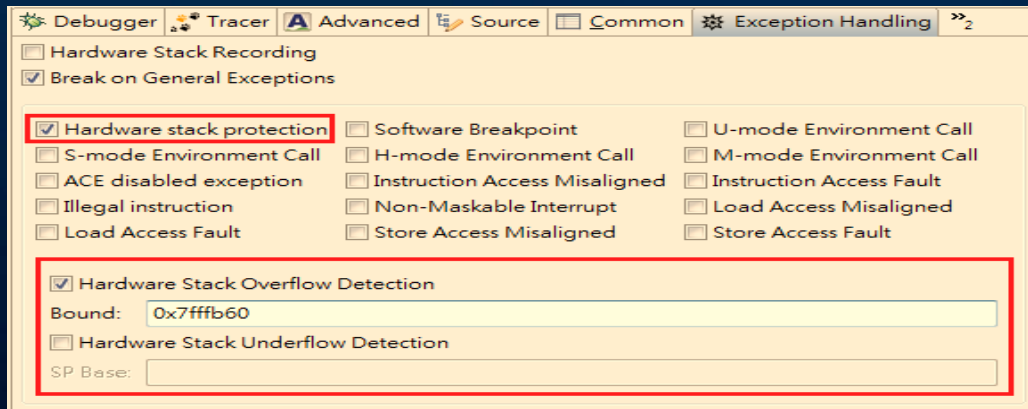
■ Record mode

- Track the maximum usage of stack pointer



■ Protection mode

- Raise an exception if over the allowed limit

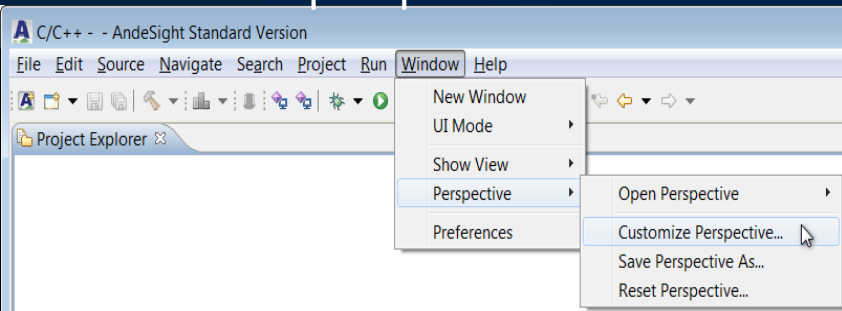




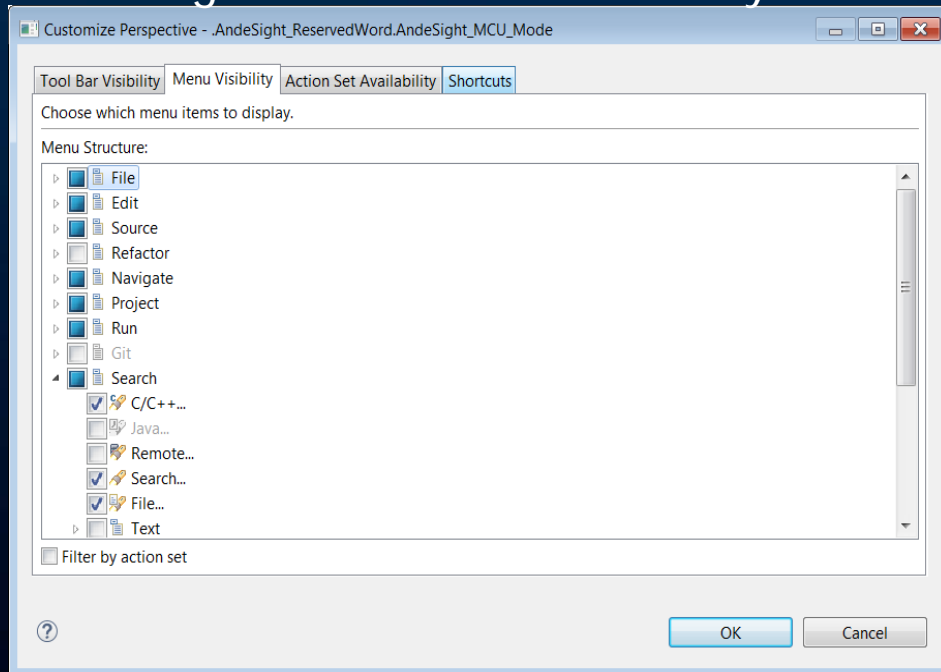
Custom UI

- Customize the layout of the Menu and Toolbar items to meet your needs

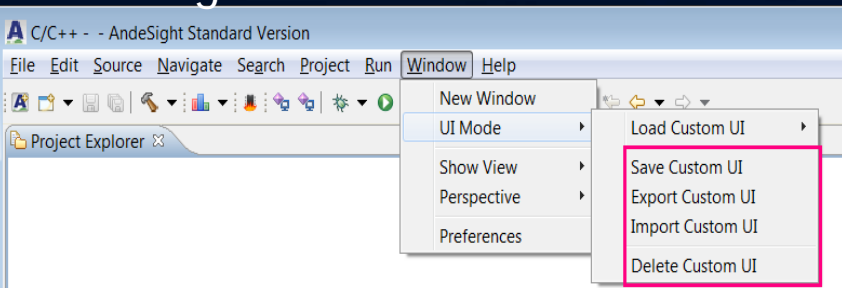
- Customize perspective



- Change menu & toolbar visibility

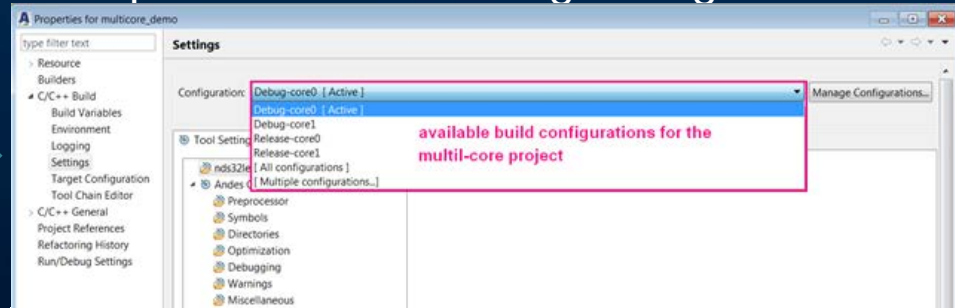
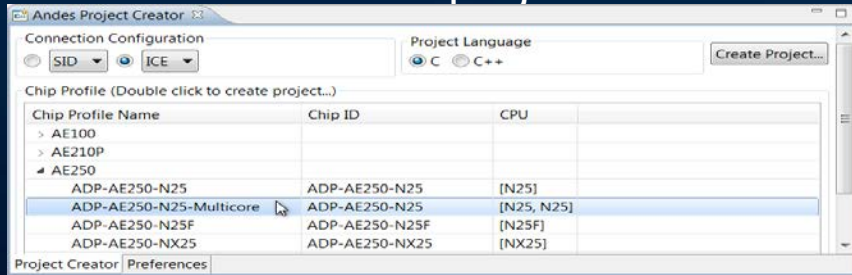


- Manage custom UI

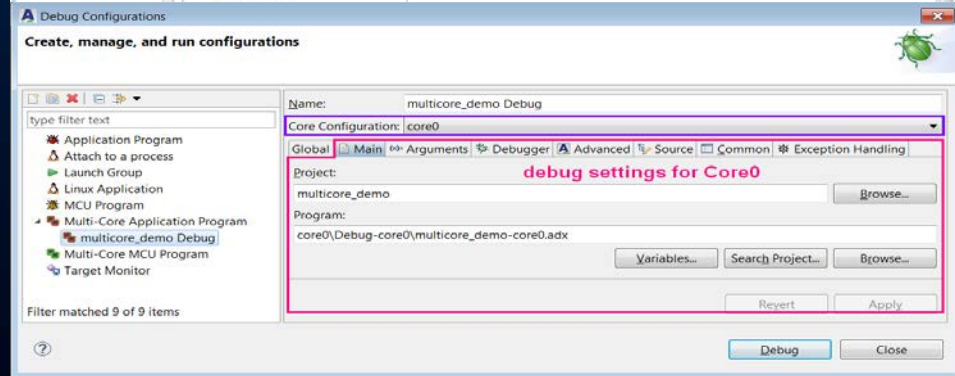
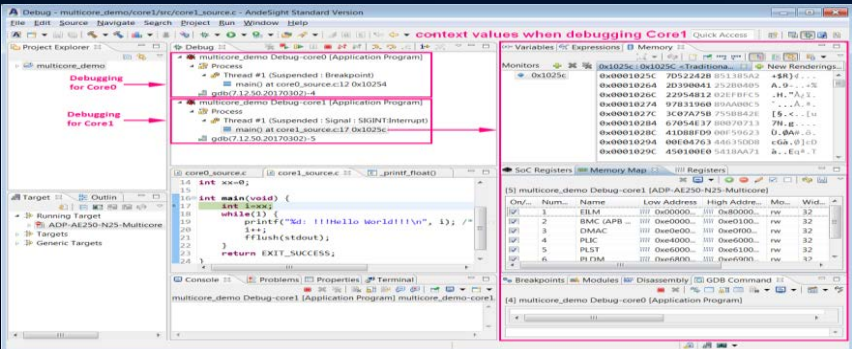


Multicore Development Support

- Develop the multicore software by simply creating multicore projects with separate build and debug configurations
- Create multicore project
- Separate build & debug configurations



- Build & debug project





Multicore Debug

AndeSight Standard Version

File Edit Source Refactor Navigate Search Project Run Window Help

Project Explorer

- demo-multicore-V5
- demo-pfm-N8
- demo-pfm-V5
- demo-plc-250-V5
- demo-plc-novector-V5
- demo-plc-V5
- demo-pmp-V5
- demo-powerbrake-V5
- demo-printf-V5
- demo-wifi-V5
- Dhrystone-V5
- Dhrystone-V5-org
- test_16cores
 - Binaries
 - Includes
 - core0
 - core1
 - core10
 - core11

Target

- Running Target
 - ADP-AE250-N25-multicore
- Targets
- Generic Targets

Debug

main() at main_core15.c:19 0xaa
gdb(8.1.50.20180309)-10
test_16cores Debug-core11 [Application Program]
Process
Thread #1 (Suspended : Breakpoint)
main() at main_core11.c:19 0xaa
gdb(8.1.50.20180309)-11
test_16cores Debug-core12 [Application Program]
Process
Thread #1 (Suspended : Breakpoint)
main() at main_core12.c:19 0xaa
gdb(8.1.50.20180309)-12
test_16cores Debug-core13 [Application Program]
Process
Thread #1 (Suspended : Breakpoint)
main() at main_core13.c:19 0xaa
gdb(8.1.50.20180309)-13
test_16cores Debug-core14 [Application Program]
Process
Thread #1 (Suspended : Breakpoint)
main() at main_core14.c:19 0xaa
gdb(8.1.50.20180309)-14
test_16cores Debug-core15 [Application Program]
Process
Thread #1 (Suspended : Breakpoint)
main() at main_core15.c:19 0xaa
gdb(8.1.50.20180309)-15

Variables Expressions Memory

Name	Type	Value
result_value	volatile int	0x126
value_array	int [15]	0x200fb0

SoC Registers Memory Map Registers

Name	Value	Description
All Registers		
General Purpose Registers		
Control and Status Registers		

Breakpoints Modules Search

- ☒ (test_16cores/core1) [address: 0x0000000000000104]
- ☒ (test_16cores/core1) main_core1.c [line: 25]

main_core1.c main_core15.c

```
17 {  
18  
19     volatile int result_value = 0;  
20     int value_array[15] = {0x10101010, 0x20202020, 0x30303030,  
21                          0x60606060, 0x70707070, 0x80808080, 0x90909090,  
22                          0xc0c0c0c0, 0xd0d0d0d0, 0xe0e0e0e0, 0xf0f0f0f0,  
23                          0x10101010, 0x20202020, 0x30303030, 0x40404040, 0x50505050};  
24 }
```

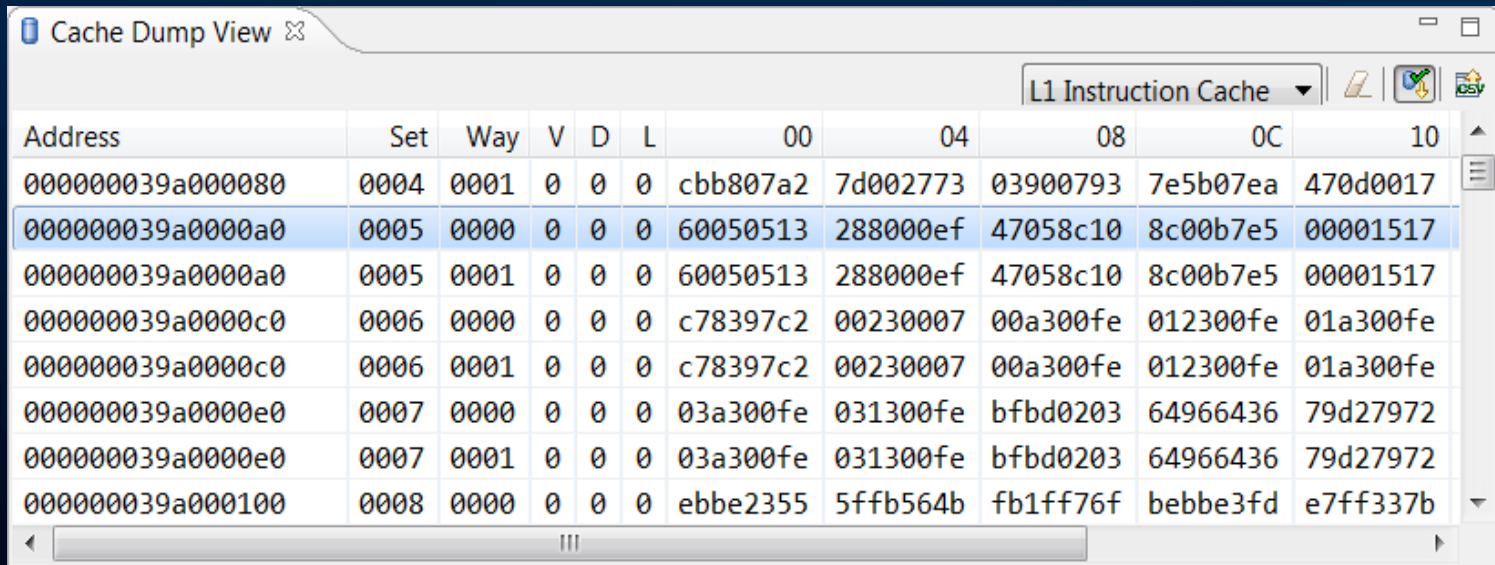
Console Problem Property Termin GDB Co Disasse

Enter location here

No details to display for the current selection.

Cache Dump View

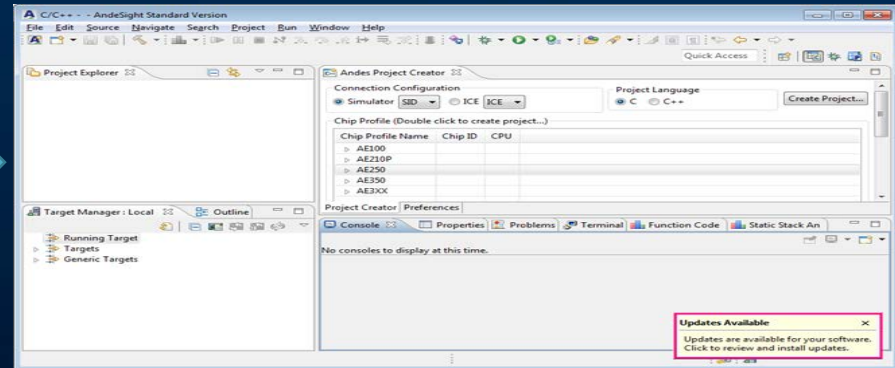
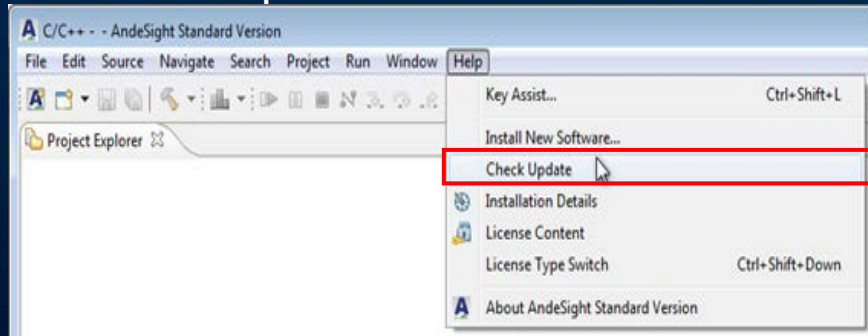
- Easily monitor CPU caches when program suspends



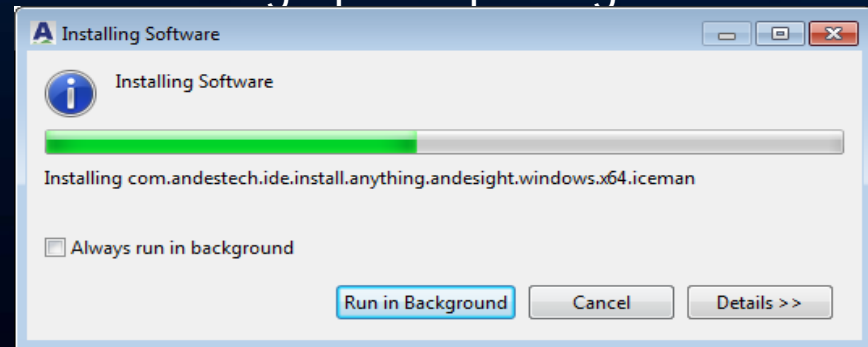
Address	Set	Way	V	D	L	00	04	08	0C	10
000000039a000080	0004	0001	0	0	0	cbb807a2	7d002773	03900793	7e5b07ea	470d0017
000000039a0000a0	0005	0000	0	0	0	60050513	288000ef	47058c10	8c00b7e5	00001517
000000039a0000a0	0005	0001	0	0	0	60050513	288000ef	47058c10	8c00b7e5	00001517
000000039a0000c0	0006	0000	0	0	0	c78397c2	00230007	00a300fe	012300fe	01a300fe
000000039a0000c0	0006	0001	0	0	0	c78397c2	00230007	00a300fe	012300fe	01a300fe
000000039a0000e0	0007	0000	0	0	0	03a300fe	031300fe	bfb0203	64966436	79d27972
000000039a0000e0	0007	0001	0	0	0	03a300fe	031300fe	bfb0203	64966436	79d27972
000000039a000100	0008	0000	0	0	0	ebbe2355	5ffb564b	fb1ff76f	bebbe3fd	e7ff337b

AndeSight Updater

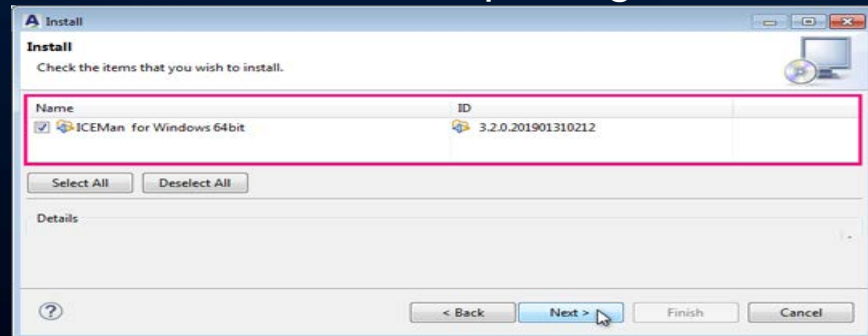
- Friendly and easy-to-use update interface
- Check update
- Notification wizard



- Installing update packages



- Select the desired packages





AndeSoft™ BSP

Bare Metal, RTOS, Linux and DSP ISA

AndeSoft™: Application Building Blocks

Fundamental

- Compiler and toolchain are contributed to and supported officially by **GNU and LLVM** communities
- Optimized **MCUlib**, newlib, glibc and **DSPLib**
- Concise linker script and its tools, **Linker Scattering-and-Gathering (LdSaG)**
- **Sample programs** to demo AndesCore™ features

Real-Time Operating Systems

- **Open source:** Zephyr, FreeRTOS
- **Commercial:** ThreadX, LiteOS, RT-Thread, SylixOS
- **RISC-V ready:** VxWorks, µC/OS-[II/III], MyNewt, embOS, RTEMS, NuttX, seL4, uC3/Compact, AliOS Things



Linux, Middleware and SW Framework

- **Linux kernel** since 4.17, device drivers and advanced features: **strace, ftrace, Perf, SMU, power throttling, suspend to RAM and kernel module**
- **U-Boot** and **BBL**
- **Andes6:** connect LPWAN to IPv6 seamlessly



AndeSoft™: Bare Metal

- Rich **startup demo** projects for Andes-specific features

Categories	Startup demo
Interrupt	PLIC, CLIC
Memory	MMU, PMP, cache, cache lock, ECC, bus matrix slave port
Power Management	PowerBrake, hibernate, WFI CPU standby/resume
Programming	DSP, printf UART redirect, C++ programming
Misc	StackSafe™, performance monitor, SMP

- **AMSI** (Andes MCU Software Interface) driver APIs
 - UART, GPIO, RTC, PWM, SPI, I2C, WDT and DMA

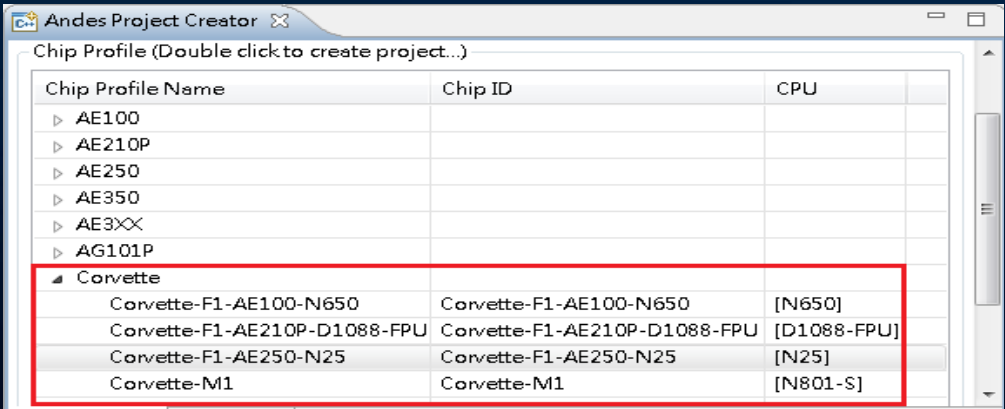


Arduino Development

- Support Arduino language reference APIs
- Support Arduino standard libraries
- AndeSight™ IDE Arduino software development plugin



AndeShape™Corvette-F1



AliOS Things



RT-Thread



SylixOS[®]
embedded



μC/OS[™]
RTOS and Stacks



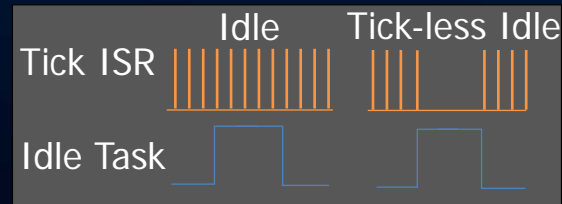
VxWorks



- A market-leading real-time operating system (RTOS) for MCU
- Scalable size, with **memory footprint** as low as 9KB
- **Tick-less idle**

➤ Power-saving by stopping periodic tick interrupt in the idle mode, supported by standard RISC-V architecture

- **AWS FreeRTOS Qualified**
- FreeRTOS test suite verified
- RTOS-awareness debugging





AndeSoft™: RTOS

- An OS that runs best on MCUs for wearable and IoT devices
- Very small **memory footprint** (will run in 8k)
- **Highly configurable, highly modular**
- Apache 2.0 license, hosted by **Linux Foundation**



- Pre-certified by TUV and UL to many **safety** standards
 - IEC-61508 SIL 4, IEC-62304 SW Safety Class C, ISO 26262 ASIL D and EN 50128
- EAL4+ Common Criteria **security** certification
- **Small footprint**, as 2KB instruction area and 1KB of RAM

- Support 32-bit/64-bit version, multicore (AMP & SMP) and **MMU**
- **Large-scale middleware** such as Qt, CODESYS, Python, Java Script and POSIX API
- **Functional safety** certified for rail transport, medical, industrial automation, automotive, electric power and aerospace



- A **Lightweight IoT Operating System** that Makes Everything Around Us Smart
- Ultra-small kernel, basic kernel size of less than 10 KB
- Low power consumption
- **One-stop software platform**, lowering development requirements and improving development efficiency
- Open Source under a BSD 3-Clause license



- An open source IoT operating system under the Apache 2.0 license
- **Abundant software components** such as GUI, TCP/IP stack, file system and standard API support like POSIX, CMSIS, C++ runtime, Javascript
- **Device and cloud integration design**, easy to connect various IoT devices with cloud

■ Linux Kernel

- LTS RV32/RV64 port, since 4.17
- SMP support
- Cache coherence and cache non-coherence support
- Linux Test Projects (LTP) verified
- Device drivers for AE350 platform

■ U-Boot

- RV32/RV64 port, maintainer and contributor
- SMP support
- Supervisor mode support
- Device drivers for AE350 platform

■ BBL





AndeSoft™: Linux

■ Linux Distribution and Build System*



*: available upon request

■ Linux Kernel Tools

- **strace/ftrace** for developers to debug
- **Perf** to evaluate the bottleneck of the whole system
- **System Management Unit (SMU)**
 - ◆ Suspend-to-RAM: suspended by sysfs and wakeup by RTC and UART interrupt
 - ◆ PowerBrake: power throttling mechanism controlled by sysfs
- **Kernel module** support all relocation types for RV32 and RV64

■ Andes GitLab Service for Linux Development Packages





Qemu

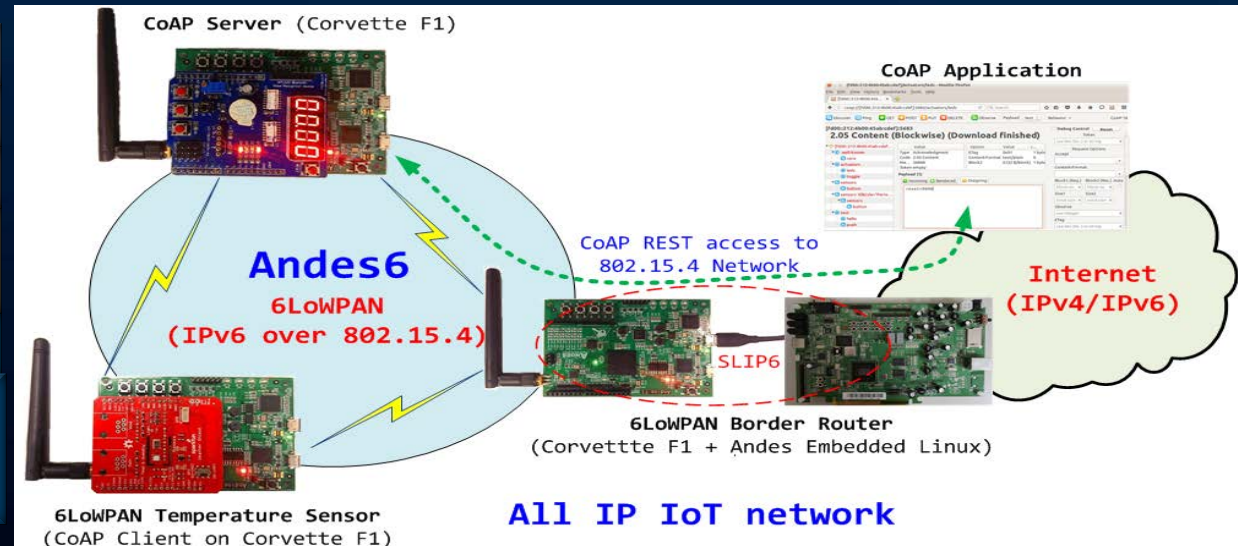
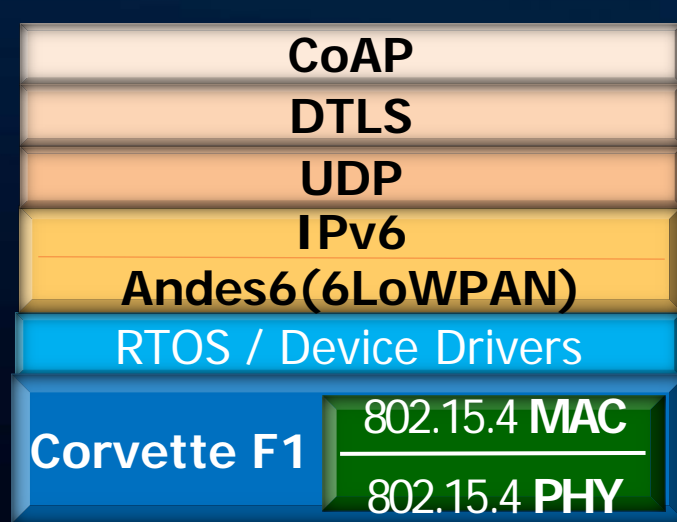
- Support AndeStar™ RISC-V V5 32/64 bits CPU
- Support AE350 SoC platform
- Integrated with AndeSight™ IDE
- Early software development and verification
 - Run U-Boot and Linux with LTP
 - Run FreeRTOS with software applications
 - Used by HPE and openSUSE project for UEFI EDKII
 - Used by Red Hat for Fedora RISC-V port regression farm





Andes6 (6LoWPAN)

- An implementation of 6LoWPAN (IPv6 over 802.15.4)
- Either third-party or open source security library can be used for security





DSP Support

■ DSP ISA assembly programming

- Derived and evolved from real use cases over decades
 - ◆ Support 32 bits and 64 bits
 - ◆ Support saturation and rounding
 - ◆ Cover SIMD, partial SIMD, bit manipulation and etc.

■ DSP intrinsic functions

- As C-like functions without bothering to program in assembly

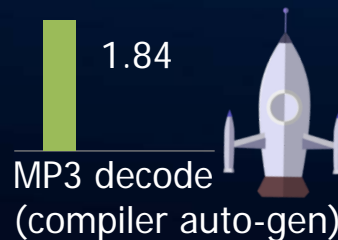
■ DSP library

- >200 functions in 8 categories (basic, complex, controller, filtering, matrix, statistics, transform and utils)

■ Some source patterns are recognized by compiler, then DSP instructions are auto-generated to facilitate development

■ Compatible with CMSIS-DSP library API

- By including an API wrapper header file



IAR Embedded Workbench for RISC-V

- Complete build and debug toolchain for RISC-V
- Support **all series of Andes RISC-V CPU**

IDE

Embedded
Workbench

Debugger

I-Jet ICE

C-SPY tool

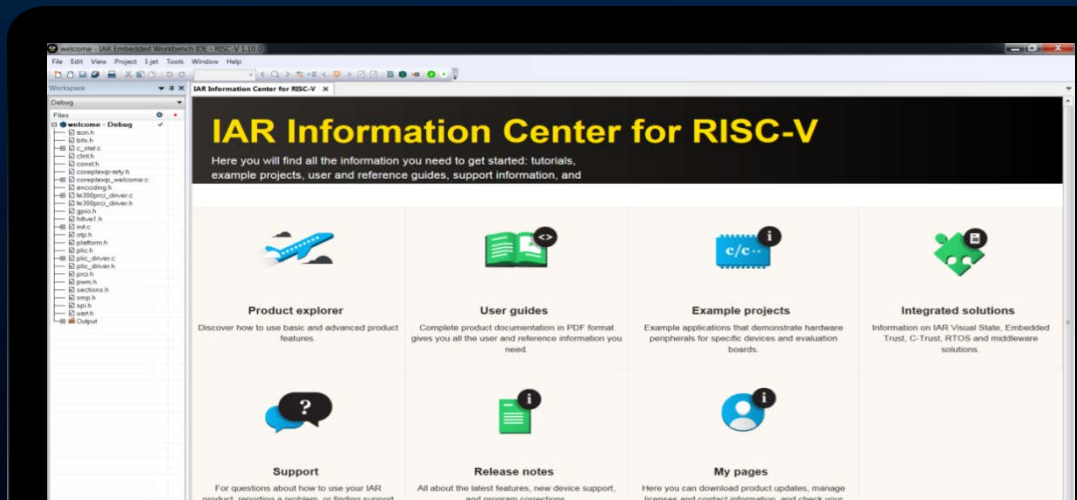
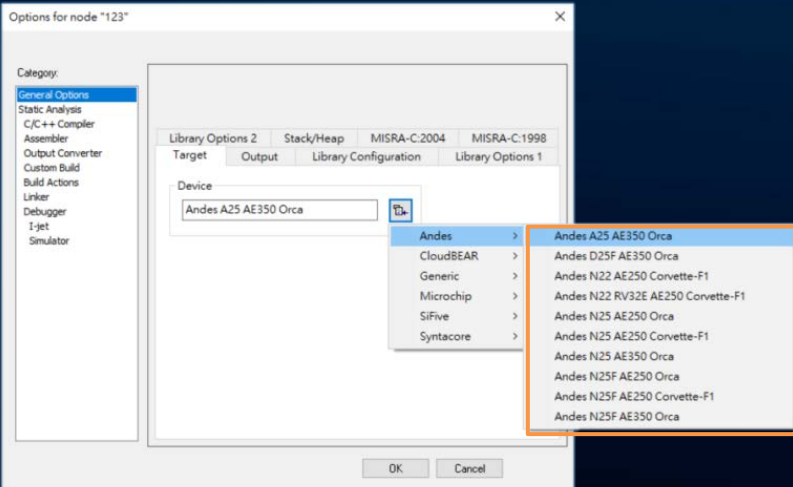


Toolchain

Compiler

C-STAT

Functional
Safety





Summary

- **AndeSight™ IDE: Rich features to speed up SW development**
 - Ease of use to reduce development time
- **AndeSoft™ BSP: Well-integrated building blocks to help users to build SoC software quickly and easily**
 - Highly-optimized toolchains for better performance and smaller memory footprint
- **Andes Comprehensive RISC-V SW solutions to achieve fast time-to-market and high quality**
 - Supporting 5 Bn+ SoC

The background of the slide is a blue-toned digital illustration. It features a wireframe hand on the left holding a square chip with the 'ANDES TECHNOLOGIES RISC-V' logo. On the right, there is a wireframe profile of a human head. The background is filled with glowing blue lines, dots, and a grid pattern, suggesting a high-tech or artificial intelligence theme.

RISC-V CON

ONLINE WEBINAR

Thank you!
See you next Webinar