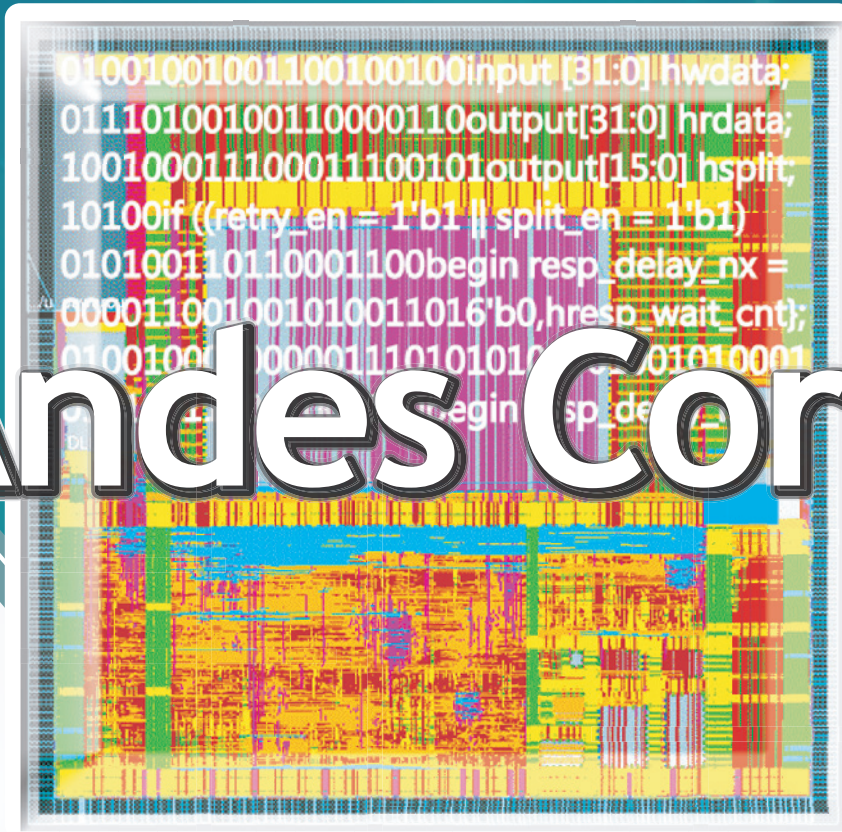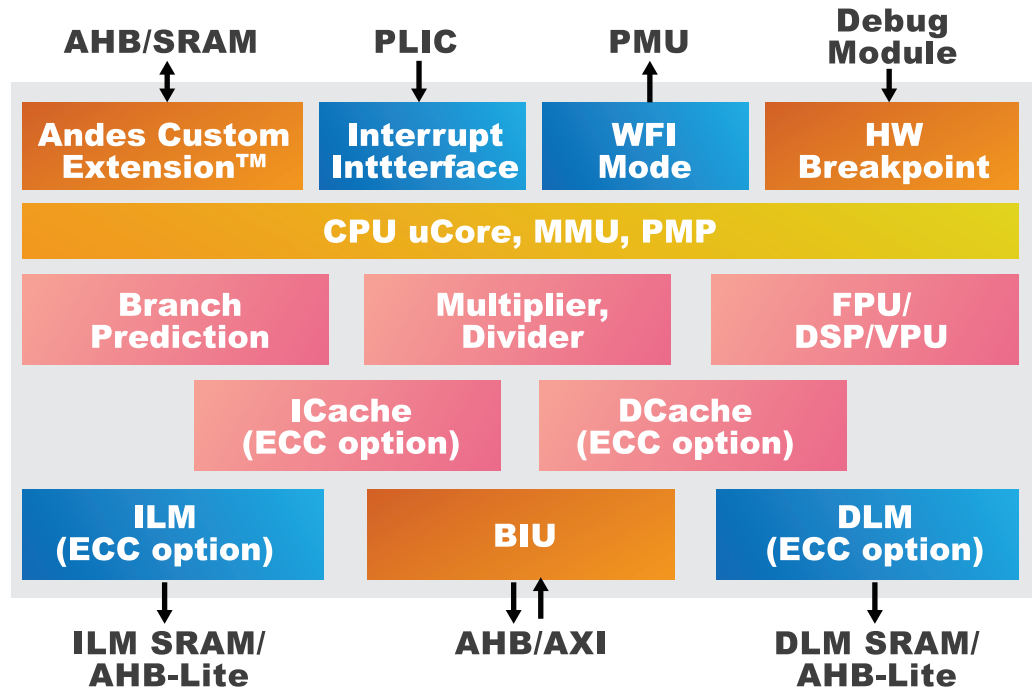# Andes Core™

ANDES
TECHNOLOGY
Driving Innovations™

RISC-V®

AndesCore™ RISC-V

AndesCore™ is a series of high performance CPU core families geared to diverse market segments of today's emerging embedded applications. The versatile and rich features of the AndesCore™ families allow flexible SoC customizations based on the application needs in a design to improve platform performance and reduce system cost. In addition, the processors employ various commonly-used low power design techniques to save energy and further allow smart SoC level power management for better energy/performance outcome.

AHB/SRAM   **PLIC**   **PMU**   **Debug Module**

Andes Custom Extension™	Interrupt Inttterface	WFI Mode	HW Breakpoint

CPU uCore, MMU, PMP

Branch Prediction	Multiplier, Divider	FPU/ DSP/VPU

ICache (ECC option)	DCache (ECC option)

ILM (ECC option)	BIU	DLM (ECC option)

ILM SRAM/ AHB-Lite   **AHB/AXI**   **DLM SRAM/ AHB-Lite**

*Availability of the above function blocks varies on each core

AndesCore™ : Performance, Power and Area

V5 Processors RISC-V	Pipeline Stage	Best DMIPS (/MHz)‰	Best CoreMark (/MHz)	Max Freq. *	Power *	Gate Count * (K)
N22 Ultra compact RISC-V core	2	1.80	3.95	700 MHz	2.42	15.8
N25F 32-bit Compact, High Performance	5	1.98	3.57	≥1.1 GHz	17	127
NX25F 64-bit Compact, High Performance	5	2.14	3.55	≥1.1 GHz	18	172
D25F 32-bit High Performance with DSP	5	1.98	3.57	≥1.1 GHz	17	186
A25 32-bit High Performance, Linux	5	1.98	3.57	≥1.1 GHz	17	144
AX25 64-bit High Performance, Linux	5	2.14	3.55	≥1.1 GHz	20	193
A25MP 32-bit Multicore, Linux SMP	5	1.98	3.57	≥1.1 GHz	#	880
AX25MP 64-bit Multicore, Linux SMP	5	2.14	3.55	≥1.1 GHz	#	1076
A27 32-bit with MemBoost, Linux	5	1.98	3.57	≥1.1 GHz	21	223
AX27 64-bit with MemBoost, Linux	5	2.14	3.55	≥1.1 GHz	23	273
A27L2 32-bit with MemBoost/L2, Linux	5	1.98	3.57	≥1.1 GHz	27	427
AX27L2 64-bit with MemBoost/L2, Linux	5	2.14	3.55	≥1.1 GHz	30	477
NX27V 64-bit with Vector Extension	5	2.14	3.55	1.2 GHz	#	#
N45 32-bit Superscalar	8	2.86	5.67	≥1.6 GHz	12.1	275
NX45 64-bit Superscalar	8	3.27	5.63	≥1.6 GHz	14.2	357
D45 32-bit Superscalar with DSP	8	2.86	5.67	≥1.6 GHz	12.1	337
A45 32-bit Superscalar Application Processor, Linux	8	2.86	5.67	≥1.6 GHz	13.5	412
AX45 64-bit Superscalar Application Processor, Linux	8	3.27	5.63	≥1.6 GHz	16.3	517
A45MP 32-bit Superscalar Application Processor, Linux	8	2.86	5.67	≥1.6 GHz	14.3	489
AX45MP 64-bit Superscalar Application Processor, Linux	8	3.27	5.63	≥1.6 GHz	16.8	632

‰ no-inline ground rules.

* 25/27 and 22 series are at 28nm. N22 configured with minimum useful configuration (small multiplier, static branch prediction). N(X)25F and D25F configured with 256-entry BTB, 16-entry PMP and 32KB L1 I/D cache, without FPU; A(X)25, A(X)25MP, A(X)27/L2 in addition with 128-entry TLB, without DSP; A(X)25MP configured with 4 cores, A(X)25MP and A(X)27L2 with 256KB L2 cache. Synthesis with 28nm process slow silicon, 0.9Vdd, 125°C with I/O constraint. Power reported at typical process corner, Vdd, 25°C. Power and gate count are core only at 1GHz. NX27V configured with VLEN=512bit and 512-bit AXI bus. Synthesis with 7nm process, 0.675v/0°C with I/O constraint, Dhrystone program. N(X)45 and D45 configured with 256-entry BTB, 16-entry PMP and PMA, and 32KB L1 I/D cache, without FPU; A(X)45/A(X)45MP in addition with 128-entry TLB. All 45-series (except A(X)45MP) data does not include FPU; A(X)45MP do not include L2 cache controller. Synthesis with 7nm FIN FET ULVT/LVT/SVT, frequency @ SSGNP 0.675v/-40°C with I/O constraint. Power reported at typical process corner, 0.75V, +85°C running Dhrystone benchmark. Power and gate count are core only @ Data are subject to change without notice. A(X)45MP power/area are for single core only.

Contact Andes for details.

AndeSight™

Software Developer's Environment

General Description

AndeSight™ is an Eclipse-based integrated development environment (IDE) which provides an efficient way to develop embedded applications for AndesCore™ based SoCs.

Features

AndeSight™

- Eclipse-based IDE
- Project management
- Managed build system
- Feature-rich editor
- Source level debugger
- Profiling analysis
- In-System programming
- RTOS awareness debugging
- Break and display on exceptions
- Register Bitfield viewing and update
- Multicore development support
- Custom UI
- AndeStar™ V5 CPU support
- Extensive demo projects
- Flexible license control
- Corvette F1 (Arduino-Compatible board) support

Toolchains

- Compiler for ELF and Linux targets
- Andes efficient ROM patch solution
- Highly optimized DSP library functions
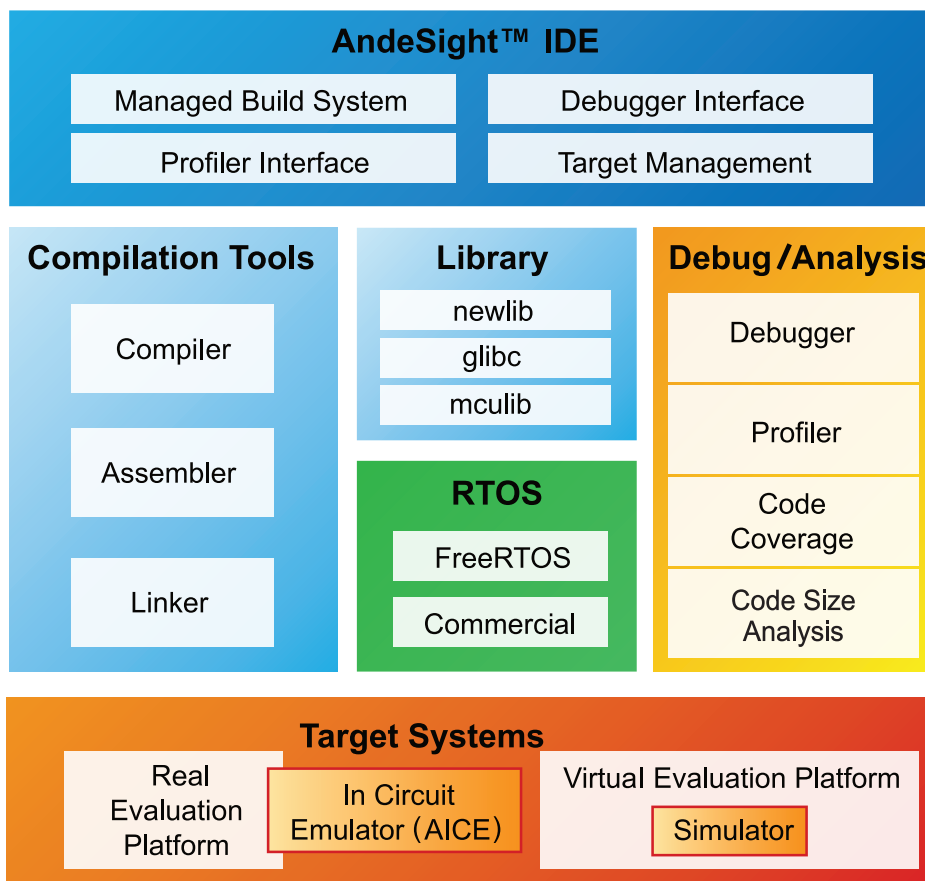- Highly optimized libc functions

Simulator

- CPU simulator(near-cycle accurate)
- Models of AndeShape™ SoC platform

ICE

- AICE debugger (4-wire/2-wire) with OpenOCD support

Supported Host Platforms

- Windows 7 / Windows 10
- Ubuntu Linux 18.04 / CentOS 7.0/ Red Hat Linux 7.0

AndeSight™ IDE

Managed Build System	Debugger Interface
Profiler Interface	Target Management

Compilation Tools
- Compiler
- Assembler
- Linker

Library
- newlib
- glibc
- mculib

RTOS
- FreeRTOS
- Commercial

Debug / Analysis
- Debugger
- Profiler
- Code Coverage
- Code Size Analysis

Target Systems

Real Evaluation Platform	In Circuit Emulator (AICE)	Virtual Evaluation Platform
		Simulator

Two AndeSight™ Versions:

STD

A comprehensive IDE with highly-optimized compilers, all GUI features, and Linux support.

RDS

Based on AndeSight™ STD with additional customization features for customers' redistribution.

AndeStar™ Architecture

The AndeStar™ V5, the latest generation of Andes architecture, consists of both 32-bit and 64-bit register architectures with mixed-length 16/32-bit instructions. It adopts the RISC-V technology as its subset and benefits from the fast growing RISC-V ecosystem. Together with the merits of performance enhancement extensions ingerited from V3, the third generation RISC-style architecture, the AndeStar™ V5 brings compact, modular and customizable advantages to SoC applications. As a founding Premier member of the RISC-V International Association, Andes is determined to take RISC-V to the mainstream.

AndeSoft™

Building Blocks for System – AndeSoft™ Software Components

With AndeSight™ IDE, users can develop software with hardware in a seamlessly integrated environment efficiently. To speed up the development process, Andes further provides a rich set of software components, from Real-Time Operating System, Linux kernel and drivers, libraries, and middleware, to application frameworks, running on AndesCore™ processors under the name AndeSoft™. Users can leverage those well-prepared and verified building blocks based on their needs and focus on tackling products to greatly improve time-to-market.

Fundamental

- Compiler and toolchain are contributed to and supported officially by **GNU** and **LLVM** communities
- Optimized C libraries: **MCUlib**, newlib and glibc
- Optimized low-level compute libraries for NN, DSP and vector processing: **libnn, libdsp, libvec**
- Concise linker script and its tools, **Linker Scattering-and-Gathering (LdSaG)**
- **Bare-metal drivers and demo programs** to demo AndesCore™ features
- Virtual platforms: **AndeSim™** (near cycle-accurate), **AndeSysC™** (SystemC library), **Qemu**

Real-Time Operating System

- Open source port on Andes: **Zephyr, FreeRTOS**
- Commercial port on Andes: **Azure RTOS ThreadX, RT-Thread, SylixOS**

aws qualified device
Amazon FreeRTOS

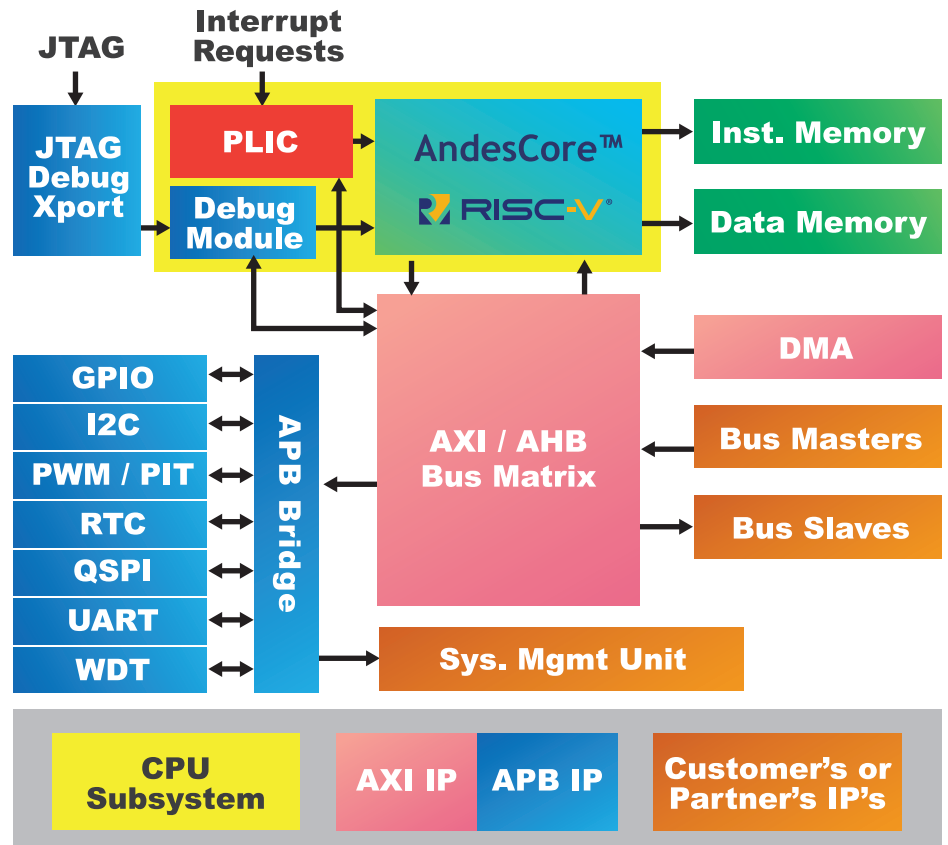### Linux, Middleware and SW Framework

- **Linux kernel** since 4.17 and LTS v5.4, device drivers and advanced features: **strace, ftrace, Perf, SMU, power throttling, suspend-to-RAM** and **kernel module**
- **U-Boot, OpenSBI** and **BBL**
- **Andes6**: connect LPWAN to IPv6 seamlessly

AndeShape™

The AndeShape™ development platform includes variety of hardware entitles, such as pre-platform IPs, ICE debuggers (AICE), and hardware evaluation boards for AndesCore™ processor based system development. To satisfy the best quality-of-result (QoR) requirements for different system applications, various platform IPs are available with different bus and datapath structures. In addition to a basic set of connectivity and storage devices, the rich set of hardware options in both board and SoC levels enable versatile flexibility in hardware/software co-development and early prototyping.

JTAG

Interrupt Requests

JTAG Debug Xport

PLIC

Debug Module

AndesCore™ RISC-V®

Inst. Memory

Data Memory

GPIO
I2C
PWM / PIT
RTC
QSPI
UART
WDT

APB Bridge

AXI / AHB Bus Matrix

DMA

Bus Masters

Bus Slaves

Sys. Mgmt Unit

CPU Subsystem

AXI IP

APB IP

Customer's or Partner's IP's

* Platform is pre-integrated with CPU
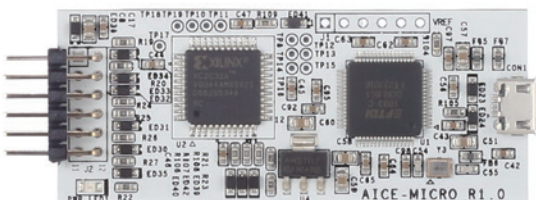* Availability of platforms varies on each core

The comprehensive debugging support, including in-system programming, self-diagnosis, and embedded ICE, greatly reduces the system development cycle while maintaining the quality of design.
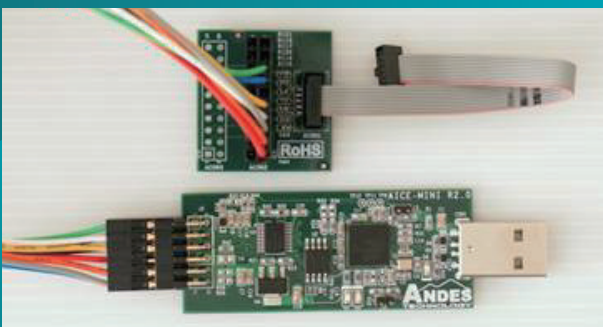
AndeShape™ AICE-MINI+
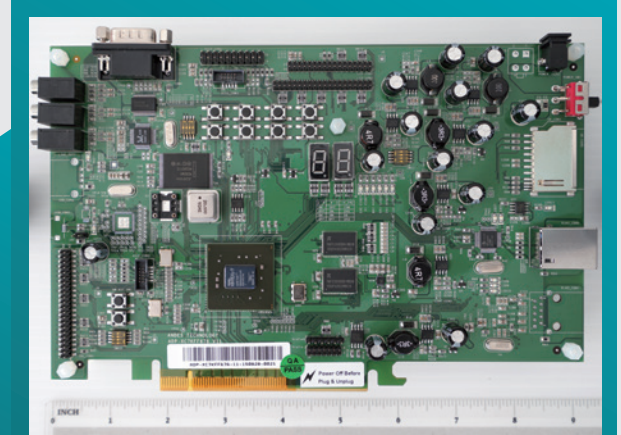
AndeShape™ ADP-XC7KFF676 EVB

AndeShape™ AICE-MICRO

![ANDES TECHNOLOGY Driving Innovations™]

About Andes Technology

Andes Technology, a Founding Premier member of RISC-V International and publicly listed CPU IP provider (TWSE: 6533; SIN: US03420C2089; ISIN: US03420C1099), has been devoting to the development of innovative high-performance/low-power 32/64-bit processors and associated SoC platforms since its foundation in 2005. Its powerful CPU lineup covering entry-level, mid-range, high-end, extensible and security families has achieved design wins in numerous embedded applications across the world, making a cumulative record of over 10 billion SoC shipment containing Andes IP as of 2021. Andes is the first mainstream CPU vendor adopting the open RISC-V. While delivering advanced features based on proprietary ISAs, Andes also provides customized CPU service. For more information about Andes' products, technologies and services, please visit www.andes-tech.com or contact us through the following.

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